IBM Field Engineering
Theory of Operation

1130 Computing System
Features

PREFACE

This manual (SY26-3670) contains information on the theory of operation of the adapter circuits for features of the IBM 1130 Computing System.

The theory of operation of the IBM 1130 Computing System is described in the IBM Field Engineering Theory of Operation, 1130 Computing System, Order No. SY26-5978.

Maintenance diagrams for the IBM synchronous communications adapter, the IBM 2501 Card Reader adapter, and the IBM 1231 Optical Mark Page Reader adapter, referenced in this manual, are in IBM Field Engineering Maintenance Diagrams, 1130 Computing System Features, Order No. SY26-4003. Maintenance diagrams for other adapters are in the IBM 1130 system logics.

Fifth Edition (October 1968, reprinted December 1970)

This is a reprint of SY26-3670-3 incorporating changes released in Field Engineering Supplement (FES) SS34-0002. Specifications contained herein are subject to change. Changes will be reported in subsequent revisions or FES's.

The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

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LIST OF ABBREVIATIONS

ACC	accumulator
BSC	binary synchronous communications
CB	circuit breaker
CCC	cycle control counter
cpm	cards per minute
cps	columns per second
CPU	central processing unit
CR	card reader
CRP	card read punch
CS	cycle steal
D/S	data set
DSW	device status word
D/T	data terminal
EA	effective address
F	format
FF	flip-flop
FL	flip latch
Hz	hertz (cycles per second)
IAR	instruction address register
ILSW	interrupt level status word
I/O	input/output
IOCC	input/output control command
lpm	lines per minute
ms	millisecond
NPRO	nonprocess runout
ns	nanosecond
Op	operation
PT	paper tape
RDR	receive deserializer register
SAC	storage access channel
SAR	storage address register
SCA	synchronous communications adapter
SP	sample pulse
SPD	sample pulse driver
SRP	serial read punch
SS	single shot
STR	synchronous transmit receive
TSR	transmit serializer register
WCA	word count address
XIO	execute I/O

INTRODUCTION

FUNCTIONS OF THE IBM 1132 PRINTER

- Provides 120 positions of output printing for the system.
- Prints numeric or alphameric information.
- Rated speed is 80 lines per minute alphameric and 110 lines per minute numeric.
- Prints 48 alphabetic, numeric, and special characters.
- Provides for forms control.
- See IBM Field Engineering Theory of Operation, 1132 Printer for additional information concerning the printer.
- Maintenance Diagrams: AA231, AA611, AA621, XP401, XP501, XP511, XP701, XP711.

The IBM 1132 Printer (Figure 1-1) provides printed output for the IBM 1130 Computing System. The rated speed is 80 lines per minute (lpm) for alphameric printing and 110 lpm for numeric printing. Actual print speeds are dependent on the program and the output format required. The print line is 120 print positions long; horizontal spacing is 10 characters per inch. Vertical spacing of six or eight lines per inch can be selected by the operator.

The 1132 contains a typewheel (Figure 1-2) with 48 alphabetic, numeric, and special characters for each of the 120 printing positions. Special characters are as follows:

& - / . $, * ( ) ' + =

Forms control is provided through a tape-controlled carriage that uses the standard IBM carriage tape. Channels 1 through 6, 9, and 12 are available to the stored program.

ADAPTER CONTROLS

- Printing and carriage operations are under direct program control of the CPU.
- The area code for the 1132 is decimal 6 (binary 00110).
- Control lines from the CPU to the adapter define the operation to be performed by the 1132 and provide timing pulses.
- Control lines from the adapter to the CPU cause cycle steal (CS) requests (level 2) and interrupt requests (level 1) when required by the 1132 printer.

The IBM 1132 Printer adapter circuits are contained within the 1131 CPU. Printing and carriage operations are started and stopped by instructions in the CPU program. Control lines from the CPU carry

Figure 1-1. IBM 1132 Printer

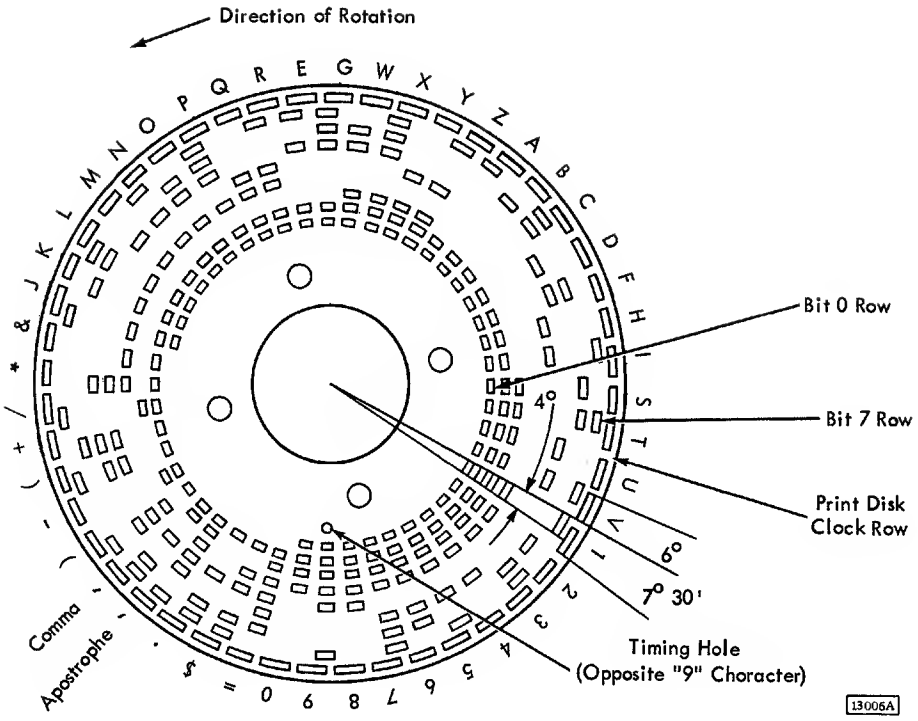


Figure 1-2. Print Disk and Typewheel

the partially decoded input/output control command (IOCC) to the adapter. This occurs at the time the CPU is executing an 'execute I/O' (XIO) instruction. Examples of such lines are 'XIO read,' 'XIO control,' and 'XIO sense device.' Activation of the 'area 6' line causes these control lines to affect the printer adapter circuits.

Other lines from the CPU further define the operation to be performed by the 1132 printer and affect adapter operation. Examples of these lines are those from certain positions of the U- and B-registers.

Once a printing operation starts, the adapter requests CS cycles and interrupts on completion of the CS cycles under control of impulses from the 1132 printer. The printer is assigned to CS level 2 and interrupt level 1. Other control lines from the adapter provide the cycle steal address, the device status word (DSW), and the interrupt level status word (ILSW) to the CPU.

PRINT OPERATION

- The program generates a print data table for one line of print.
- The program compares each character in the table with a character emitted by the printer and sets the printer scan field.
- The printer scan field is transferred to the adapter print buffer during CS cycles initiated by print disk clock pulses. Each word, while in the print buffer, causes energization of a group of print magnets in the 1132.
- The program compares each character in the data table with the next emitted character from the printer and sets the printer scan field for that character.
- The comparison of characters and transfer of the printer scan field is repeated until all desired characters have been printed.
- An instruction stops the print operation.

Characters are printed by the 1132 as a result of energizing the print magnets in the 1132. Attracting the armature of a magnet starts mechanical motion which prints a character. The position of the continuously running typewheel when print motion starts determines the character that is printed.

Print operations can vary because they are so highly dependent on the CPU program. A typical operation is described here, including a general description of the instructions and programming required.

Data Table

The data to be printed is assembled (in any unassigned core storage area)in the same order, including blanks, as the line to be printed. Usually, two characters are stored in one core storage location, and the table occupies 60 consecutive core storage locations (Figure 1-3). All characters must be stored in the 1132 printer code (Figure 1-4).

Sense DSW

Before starting the print operation, the status of the 1132 is checked. An XIO instruction, with an IOCC specifying area 6 and a function of sense device, causes the adapter to set the DSW in the CPU accumulator. The instruction must not reset any responses that are active. The program analyzes the DSW to ensure that neither the printer nor the carriage is busy and that the printer is ready.

Start Printer

An XIO instruction, with an IOCC to start printer, activates adapter circuits to sense the next print disk clock pulse from the 1132. This timing pulse causes CS requests for 16 successive CPU cycles. During these cycles, the eight words of the printer scan field are set into the print buffer, one at a time. The printer scan field is in the reserved addresses, /0020 to /0027, inclusive. Each word stays in the adapter buffer register for nearly two CPU clock cycles during the transfer (scan).

First Scan

While each word of the printer scan field is in the buffer register, print magnets are energized for positions containing 1's. The first word (from /0020) controls print positions 1-16; the second word (from /0021) controls print positions 17-32, etc.

During the first scan of a print operation, the printer scan field should contain no 1's that can cause printing. No printer emitter character has yet been read and compared with the data table. However, position 15 of the word from address /0027 must contain a 1 to prevent a print scan check. Before the first scan, the program must clear the printer scan field and set the 1 in the last position.

Read Emitter Interrupt

At the end of the printer scan field transfer (16 CS cycles), the adapter circuits cause a read emitter interrupt (printer level 1 interrupt request). The level 1 interrupt servicing subroutine must include an instruction to determine which of the level 1 devices caused the interrupt. An XIO with a function code of sense interrupt sets the ILSW into the CPU accumulator for analysis by the program.

When the program determines that the 1132 requested the interrupt, program execution branches to the 1132 portion of the level 1 interrupt servicing subroutine. An XIO instruction with an IOCC to read the printer emitter is in the level 1 interrupt servicing subroutine. Execution of this instruction sets the bit configuration of the character presently available from the 1132 emitter into core storage.

Setting Printer Scan Field

The program compares the emitter character with each character in the print data table. For each equal comparison, the program sets a 1 in the corresponding position of the printer scan field. To indicate that the complete scan field has been set, the last step is setting a 1 in position 15 of location /0027.

For correct operation, the setting of the printer scan field must be completed before the next print disk clock pulse from the printer. If it is not completed, no 1 is set in the last position of the last word of the printer scan field. Then a print scan check is indicated when the word is transferred to the printer.

Second and Succeeding Scans

Each timing pulse from the 1132 starts another scan until a program instruction stops the sensing of printer timing pulses. Each scan transfers the printer scan field for a single character and, after the transfer of the last word, causes a level 1 interrupt request. Then the program reads the printer emitter again and starts setting the printer scan field for another character. A scan is required for each character that is to be printed in one or more positions. All positions printing the same character have their print magnets energized during the same scan.

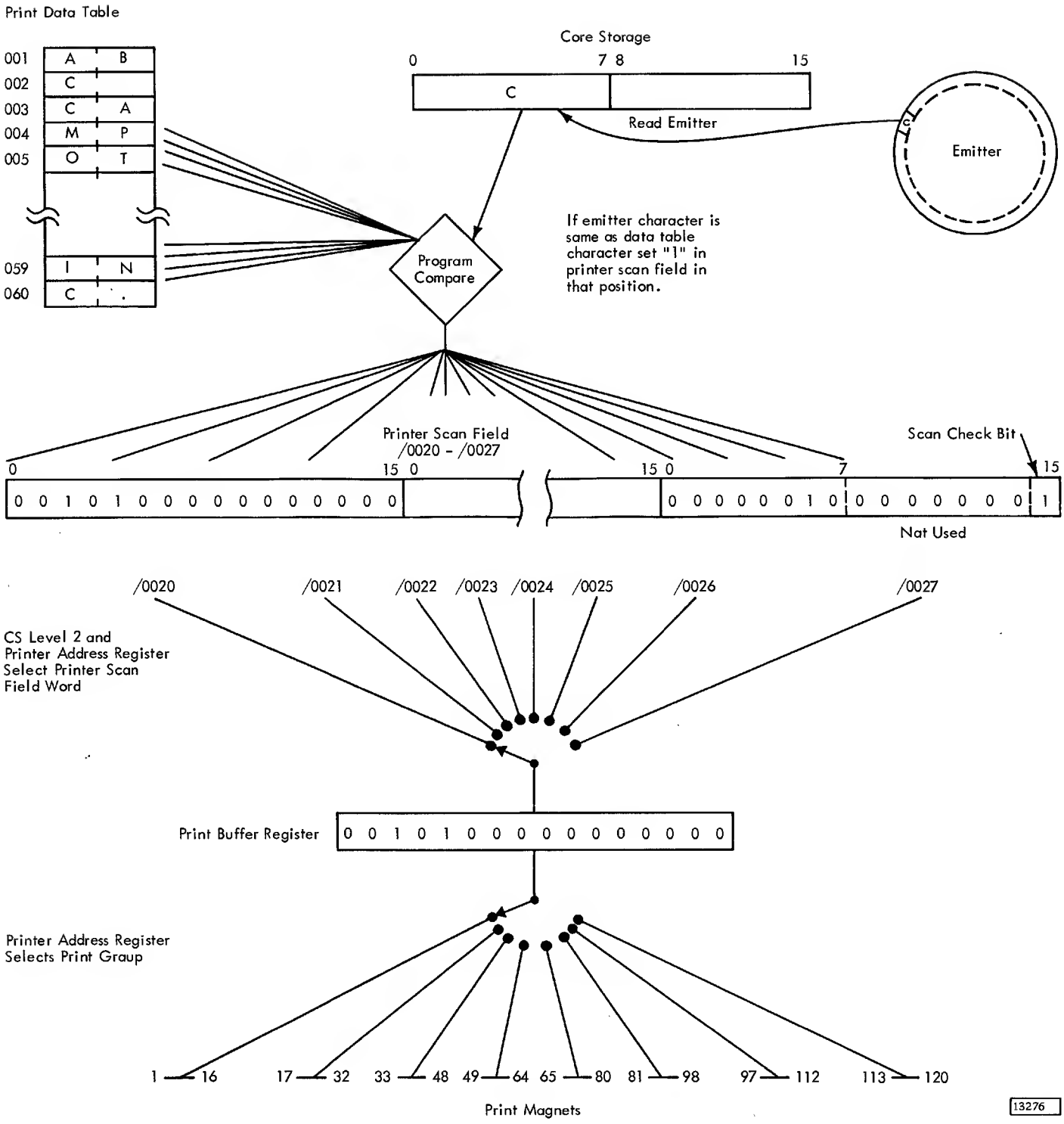


Figure 1-3. Print Operation

Character	Hex	I/O Bus Bits							
		0	1	2	3	4	5	6	7
A	C1	1	1	0	0	0	0	0	1
B	C2	1	1	0	0	0	0	1	0
C	C3	1	1	0	0	0	0	1	1
D	C4	1	1	0	0	0	1	0	0
E	C5	1	1	0	0	0	1	0	1
F	C6	1	1	0	0	0	1	1	0
G	C7	1	1	0	0	0	1	1	1
H	C8	1	1	0	0	1	0	0	0
I	C9	1	1	0	0	1	0	0	1
J	D1	1	1	0	1	0	0	0	1
K	D2	1	1	0	1	0	0	1	0
L	D3	1	1	0	1	0	0	1	1
M	D4	1	1	0	1	0	1	0	0
N	D5	1	1	0	1	0	1	0	1
O	D6	1	1	0	1	0	1	1	0
P	D7	1	1	0	1	0	1	1	1
Q	D8	1	1	0	1	1	0	0	0
R	D9	1	1	0	1	1	0	0	1
S	E2	1	1	1	0	0	0	1	0
T	E3	1	1	1	0	0	0	1	1
U	E4	1	1	1	0	0	1	0	0
V	E5	1	1	1	0	0	1	0	1
W	E6	1	1	1	0	0	1	1	0
X	E7	1	1	1	0	0	1	1	1
Y	E8	1	1	1	0	1	0	0	0
Z	E9	1	1	1	0	1	0	0	1
0	F0	1	1	1	1	0	0	0	0
1	F1	1	1	1	1	0	0	0	1
2	F2	1	1	1	1	0	0	1	0
3	F3	1	1	1	1	0	0	1	1
4	F4	1	1	1	1	0	1	0	0
5	F5	1	1	1	1	0	1	0	1
6	F6	1	1	1	1	0	1	1	0
7	F7	1	1	1	1	0	1	1	1
8	F8	1	1	1	1	1	0	0	0
9	F9	1	1	1	1	1	0	0	1
=	7E	0	1	1	1	1	1	1	0
$	5B	0	1	0	1	1	0	1	1
.	4B	0	1	0	0	1	0	1	1
'	7D	0	1	1	1	1	1	0	1
,	6B	0	1	1	0	1	0	1	1
(	4D	0	1	0	0	1	1	0	1
-	60	0	1	1	0	0	0	0	0
)	5D	0	1	0	1	1	1	0	1
+	4E	0	1	0	0	1	1	1	0
/	61	0	1	1	0	0	0	0	1
*	5C	0	1	0	1	1	1	0	0
&	50	0	1	0	1	0	0	0	0

BR0273

Figure 1-4. Printer Code

The program determines how many scans occur. If there is a possibility that all 48 characters could appear in a line of print, 48 scans must occur. If only numeric characters are to be printed, fewer scans are required. In any case, the program must ensure that every print position has been given the chance to print all the desired characters.

Stop Printer

When all the required scans have been completed, the printer can be instructed to stop. An XIO instruction, with an IOCC to stop printer, prevents the adapter from sensing any more print disk clock pulses.

If a space or skip operation is to follow the print operation, the program must provide additional time to complete the mechanical operation of printing the last character. After the final scan for a line of print, the program must provide 16 idle scans before stopping the printer and starting the space or skip. These idle scans are like the first scan, with the printer scan field set to 0's, except for bit 15 of the eighth word (location /0039).

CARRIAGE OPERATIONS

- Carriage operations advance the forms one line (space) or multiple lines (skip).
- Carriage operations are started by XIO instructions. Different IOCC's cause space or skip operations.
- Carriage timing pulse stops a space operation.
- Program stops a skip operation.
- Space and restore operations can be caused by manual controls on the 1132 printer.

The operations that can be performed by the carriage, under control of the adapter, are:

1. Manual or programmed space (one line at a time).
2. Programmed skip (multiple lines).
3. Manual restore (one or more lines to a predetermined line).

Space Operation

The forms can be advanced a single line either by executing an instruction or by pressing the carriage

space pushbutton switch on the printer. Either method activates adapter circuits to engage the carriage drive clutch.

A timing pulse from the carriage deactivates the adapter circuits to stop the motion. A carriage space interrupt occurs at this time, if the space operation was the result of an instruction. No interrupt is caused by a manual space, and no manual space can occur during a print operation.

Skip Operation

A skip operation requires an instruction to start and an instruction to stop. After paper motion starts, each hole in the carriage control tape sensed by a carriage brush causes the adapter to request a level 1 interrupt. The program must determine whether or not the hole that is being sensed should stop the carriage. The program issues the stop command when the forms have been advanced the desired distance.

Restore Operation

Pressing the carriage restore pushbutton switch starts a restore operation. The carriage runs until the carriage brush for channel 1 senses a hole in the carriage control tape. No interrupt occurs for this manual operation.

PROGRAMMING NOTES

The status of the 1132 should be checked before the first line of a record is printed. This is accomplished by sensing the printer DSW. The modifier bits of the sense device instruction should be set to 0's to prevent reset of the DSW responses and indicators. Bits 3, 5, and 6 of the DSW are tested and if all three positions contain 0's, the printer is ready to print the next line. A printer start control command is then given to start the timing sequence. A scan field transfer, using cycle steal cycles, takes place under control of the printer. Therefore, the scan field must be clear and have a 1 set in bit 15 of word 0039 by the program before the printer start command is given.

At the end of the scan field transfer, a level 1 interrupt occurs. The code of the next character is available from the emitter and is read into core storage by a read emitter instruction. There are approximately 11.2 ms available for the program to compare each position of the output record with the emitter character and set up the printer scan field. At the next print disk clock pulse, the printer adapter begins its scan and fires each print magnet having a corresponding 1 in the printer scan field. If the program has been interrupted for a considerable time by higher levels, the programmed scan may not have been completed. To ensure that the program detects this condition, the first steps of the printer subroutine for each character should clear the printer scan field to 0's and, upon completion of the programmed comparison, place a 1 in position 15 of the eighth word (/0027). When the printer adapter scans the field it checks this position. If it is 0, the print scan check indicator (bit 4 of the DSW) is turned on. The program can test this position and branch to an error routine that provides 47 idle scan cycles and resumes programmed scanning at the point where the scanning was interrupted. This results in overprinting of the characters that were previously printed unless the error routine keeps track of the positions that had been printed and does not set them up again on this scan.

After the final character scan cycle for a line of printing, 16 idle scan cycles must be taken before spacing or skipping is started. Doing so allows time for completion of the mechanical operation of printing the last character. If the operation is a space, the next scan cycle can be started two scan cycles after the last space command is given.

During an idle scan cycle the printer scan field should be set to 0's. Bit 15 of the eighth word (/0027), however, is set to 1 to prevent the print scan check indicator from being turned on.

FUNCTIONAL UNITS

The functional units in the 1132 printer adapter are used in transferring data and energizing print magnets during CS cycles. They are the printer address register and the print buffer register.

PRINTER ADDRESS REGISTER

- Register contains three flip-flops and acts as a binary counter.
- Printer being stopped resets all flip-flops to the off side.
- Register outputs assist in selecting a word from the printer scan field during CS cycles.
- Register activates lines to the 1132 printer to select groups of print magnets.
- Contents are stepped every other CS cycle.

- After the last word of the printer scan field is transferred, the register output prevents further CS requests.

The printer address register is reset (all flip-flops off) by a power on reset. It is also returned to this condition by the 'CPU stop' latch or an instruction to stop the printer. When gated, an 'X6' pulse can change the state of the 'printer address register bit 1 FF. Turning off the 'bit 1' FF changes the state of the 'printer address register bit 1' FF. The 'bit 2' FF controls the 'printer address register bit 4' FF in the same manner. Thus, the register acts as a binary counter.

Changing Value in the Register

Stepping of the register is gated by 'CS level 2' and 'printer CS control' lines. 'Printer CS control' is the output of the 'CS control' FF, which changes state at the end of every 'X6' pulse when 'CS level 2' is active. Therefore, the value in the register is stepped during the 2nd, 4th, ... 12th, and 16th CS cycles. The last (eighth) step returns the value to 0, with all flip-flops off.

Addressing CPU Core Storage

Each flip-flop, when it is on, activates a line to the CPU for use in addressing core storage during the printer CS cycles. In the CPU circuits, 'CS level 2' activates the 'printer address 10' line, which alone addresses /0020 location. 'CS level 2' also ANDs with the outputs of the three 'printer address register' flip-flops when they are on. Together, these lines provide an address from /0020 to /0027, inclusive, for each CS level 2 cycle.

Print Group Selection

The outputs of the register flip-flops enter logic to activate one of the 'print select group 0' to 'print select group 7' lines. These lines to the 1132 each gate one group of 16 print magnets (except for group 7, which has only eight print magnets).

'Print select group 7' has additional functions. This line active and no 1 in B-register bit 15 position gate the turn-on of the 'print scan error' FF. This line also gates the turnoff of the 'CS request' FF at the end of X4 of the last CS cycle.

PRINT BUFFER REGISTER

- Register consists of 16 flip-flops.
- Loading with successive words from the printer scan field occurs every other CS cycle.
- Output enters 1132 printer logic to determine which of the selected group of print magnets are to be energized.

The flip-flops of the print buffer register provide temporary storage in the adapter for words of the printer scan field. When a word is in the register, print magnets in the 1132 are energized for those register positions that contain 1's.

The print buffer register is reset (all flip-flops turned off) by a power on reset. 'CS level 2' and an 'X4' pulse activate the 'load print buffer' line if the 'CS control' FF is off. The flip-flops of the buffer register are set to match the flip-flops of the B-register in the CPU. The word remains in the print buffer register until it is reset at X6 of the next CS cycle (Figure 1-5).

PRINCIPLES OF OPERATION

- All programmed operations are started by XIO instructions in the CPU.
- Area code (in the IOCC) for the 1132 printer is decimal 6 (00110).

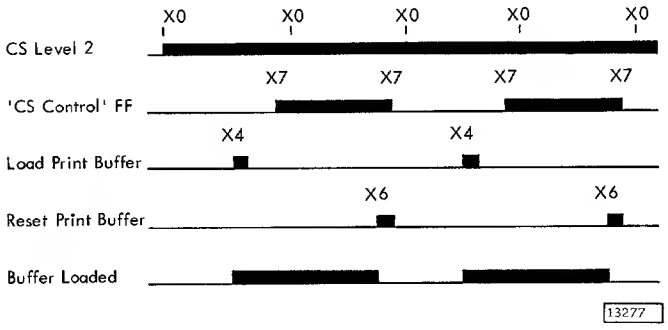


Figure 1-5. Print Buffer Register

- Function code and modifiers (in the IOCC) define the adapter and device operation to be performed. performed.

The operation of the adapter circuits depends on the decoding of the IOCC that is read from storage.

SENSE INTERRUPT (011)

- Sense interrupt function code causes the setting of the ILSW in the CPU A-register.
- The ILSW for the interrupt level being serviced when the instruction is given in the ILSW that is set.
- Only the function code (011) is required in the IOCC.
- The program uses the ILSW to determine the device (area code) which caused the interrupt.

A function code of sense interrupt activates the 'XIO sense ILSW' line. 'Printer level 1 interrupt request' is activated by the adapter when one of these flip-flops is on:

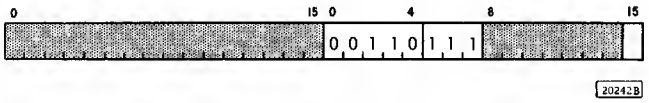
'Read emitter interrupt' FF.
'Carriage skip interrupt' FF.
'Carriage Space interrupt' FF.

The aforementioned lines being active, while the 'interrupt level 1' line is active, activates 'printer ILSW bit 0.' The result is setting a 1 in B-register bit 0 position during the E2 cycle of the operation. The 1 is transferred to the A-register via the D-register. It is not, however, written into core storage, because 'storage use' is blocked in this cycle.

SENSE DEVICE (111)

- Sense device function code causes the setting of the DSW in the CPU A-register.
- Status of the 1132 should be checked before the 1132 is given an instruction to start.
- DSW is also analyzed in the interrupt level 1 servicing subroutine.

An XIO instruction with the sense device function code, given before the printer is started, sets the printer DSW into the CPU accumulator for program analysis. The IOCC must not contain the bits to reset the indicators in the DSW at this time. The IOCC for this operation follows.



The DSW for the printer is shown (Figure 1-6).

Significance of DSW Bits

Read Emitter Response (Bit 0): This position is set to a 1 when the 'read emitter interrupt' FF is on when the sense device occurs. The 'read emitter interrupt' FF is turned on by turning off the 'CS request' FF at the end of the printer scan field transfer. A 'Bbit 0' is required to turn off the 'read emitter interrupt' FF (see "Sense Reset").

Skip Response (Bit 1): A 1 in this position indicates that the 'carriage skip interrupt' FF is on. This flip-flop is turned on each time a hole in the carriage control tape is sensed while the 'skip start latch' is on. A 'B bit 1' is required to turn off the 'carriage skip interrupt' FF (see "Sense Reset").

Space Response (Bit 2): A 1 in this position indicates that the 'carriage space interrupt' FF is on. This flip-flop is turned on when the 'carriage CB' line is activated and turns off the 'line space latch.' A 'B bit 2' is required to turn off the 'carriage space interrupt' FF (see "Sense Reset").

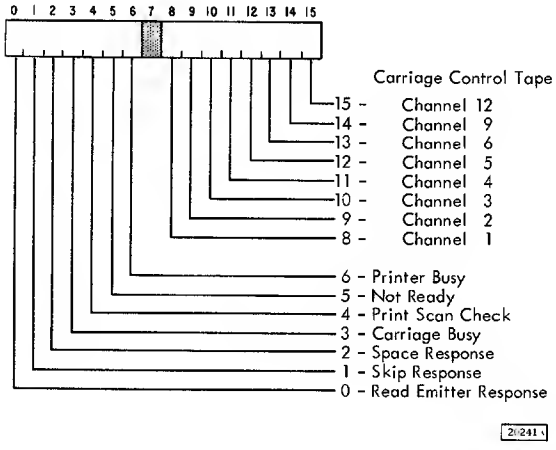


Figure 1-6. Device Status Word (1132 Printer)

Carriage Busy (Bit 3): A 1 in this position indicates that the carriage is spacing or skipping and that one of the following lines is active when the sense device operation occurs:

1. 'Skip start latch,' indicating that flip-flop is on.
2. 'Carriage magnet select,' indicating the carriage magnet is energized.
3. 'Interposer contact,' indicating the interposer contact is closed.
4. 'Space carriage busy,' indicating the 'line space latch' is on.

Print Scan Check (Bit 4): A 1 in this position indicates that the 'print scan error' FF is on. This flip-flop is turned on when the last word of the printer scan field is gated to the print buffer, if the 'B bit 15' line is not active. The flip-flop turning on indicates an error in setting or transferring the printer scan field. A print scan error does not cause an interrupt. However, a 'B bit 4' is required to turn off the 'print scan error' FF.

Not Ready (Bit 5): A 1 in this position indicates that the 'ready' latch is off. The 'ready' latch is turned on when forms are in place in the carriage, the motor switch is on, and the start key is pressed. Pressing the stop key turns on the 'stop' latch and with the 'run' latch off, turns the 'ready' latch off.

If the forms contact transfers, indicating there are no more forms, the 'ready' latch turns off the next time the 'run' latch turns off. Also, if the 'run' latch is on when the stop key is pressed, the 'ready' latch turns off when the 'run' latch does.

Printer Busy (Bit 6): A 1 in this position indicates that the 'run' latch is on. The 'run' latch is turned on by an XIO instruction if the 'ready' latch is on. It can be turned off by another XIO instruction, or by activating the 'CPU stop latch' line or the 'printer DC reset' line.

Channels 1-6, 9 or 12 (Bits 8-15): A 1 in any of these positions indicates that the corresponding carriage brush is reading a hole punched in the control tape, as shown in Figure 1-6.

Sense Reset

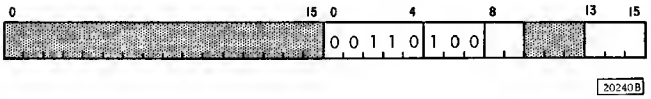
The sense device function is also programmed during the interrupt level 1 servicing subroutine. In this case, the IOCC usually contains a 1 in position 15 of the control (second) word. The 'U bit 15' with 'XIO sense device' and 'T6' in the CPU activate the 'XIO sense reset 15' line to the adapter. The result is that the condition in the adapter that caused the interrupt is turned off.

The reset of the interrupt condition, described in the previous paragraph, also depends on the presence of a 1 in the corresponding position of the B-register. This requirement ensures that the 1 was set in the B-register by the sense DSW. For example, to reset the 'read emitter interrupt' FF, there must be a 1 in the bit 0 position of the B-register. The sense device operation sets the DSW in the B-register before transferring the DSW to the A-register.

CONTROL (100)

- Control function code sets up adapter circuits to perform operations further defined by the modifier bits in the IOCC.
- The adapter circuits use the output of the U-register to further define the operation to be performed.

The IOCC for control functions as applied to the 1132 printer is:



Modifier bits 8, 9, and 13-15 define the operation that is to be performed by the XIO control function. The address word of the IOCC is not used. Decoding the IOCC control word in the CPU U-register activates the 'XIO control' line to the adapter during E2.

Start Printer

- Modifier bit 8 = 1 causes the start printer control function.
- Start printer sets the adapter circuits so that the next print disk clock pulse starts CS cycles.
- Sixteen CS cycles and an interrupt request result from each print disk clock pulse until the stop printer instruction.
- Maintenance Diagram XP501.

'XIO control' from the CPU is active during the E2 cycle, and 'U reg 8' turns on the 'run' latch at T6. The 'run' latch being on:

1. Activates 'print gate' to device circuits.
2. Sets the printer busy bit in the DSW.
3. Blocks the turn-on of carriage control latches.
4. Turns on the 'use meter' latch.
5. Gates the turn-on of the 'CS request' FF.

The end of each 'print disk clock' pulse, received from the printer device circuits, starts a 4-ms singleshot. When the singleshot times out, the voltage shift turns on the 'CS request' FF, if 'printer run latch' is active.

'CS request' remains on while 16 CS cycles are taken by the CPU. The printer address register steps every other CS cycle and addresses CPU core storage. The printer address register also selects (gates) groups of print magnets in the 1132. During the last CS cycle, 'print select group 7', 'CS level 2', and 'CS control' FF on activates a gate that allows 'X4' to turn off the 'CS request' FF.

When the 'CS request' FF turns off, the voltage shift turns on the 'read emitter interrupt' FF. This flip-flop being on sets a 1 in the DSW bit 0 position if the DSW is sensed. The 'read emitter interrupt' FF being on is also one of the ways to activate 'printer level 1 interrupt request.' In the servicing subroutine, the program must read the emitter character, compare, and set the new printer scan field.

The 'run' latch stays on until turned off by a later XIO control function. Each succeeding 'print disk clock' pulse, meanwhile, turns on the 'CS request' FF for a print scan.

Stop Printer

- Modifier bit 9 = 1 causes the stop printer control function.
- The CPU program determines when no more printer emitter pulses should be recognized. (The required number of scans has been completed.)
- The stop printer function is not usually programmed until the idle scans have been completed. (Idle scans are necessary to allow time after printing before space or skip operations.)
- Maintenance Diagram XP501.

'XIO control,' 'area 6,' and 'U reg 9' from the CPU combine to turn off the 'run' latch at T6. Following emitter pulses from the 1132 printer no longer causes CS cycles and interrupts. The printer busy bit is not set when the DSW is sensed. Carriage function latches can be set.

Start Carriage

- Modifier bit 13 = 1 causes the start carriage control function.
- Start carriage engages clutch so drive motor drives carriage mechanism, moving forms.
- Program must stop motion when required.
- Maintenance Diagram XP511.

'XIO control,' 'area 6,' and 'T6' activate 'printer control load.' This line and 'U reg 13' being active turn on the 'skip start' latch, which activates 'interposer magnet select' to the 1132 circuits. When the interposer contact in the device activates the adapter 'interposer contact' line and the 'skip start' latch is on, 'carriage magnet select' energizes the clutch magnet in the 1132. Carriage and forms motion start.

A later instruction in the program is required to stop the skip operation.

Stop Carriage

- Brushes 1-6, 9, and 12 activate the corresponding lines in the adapter when they sense holes in the carriage control tape. Any one turns on the 'carriage skip interrupt' FF.
- Program analyzes the DSW to determine whether or not carriage skip operation should stop.
- Modifier bit 14 = 1 causes the stop carriage control function.
- Stop carriage turns on the 'skip stop latch' when the 'carriage CB' line from the 1132 is active.
- Carriage clutch disengages, and forms movement stops.
- Maintenance Diagram XP511.

While the forms are feeding, carriage brushes 1 through 6, 9, or 12 can sense holes in the carriage

control tape. Sensing any hole activates the corresponding 'carriage brush' line and the 'any carriage channel' line. If the carriage has started a skip operation that is not a (manual) restore operation, the turn-on of the 'carriage skip interrupt' FF is continuously gated. Activating 'any carriage channel' while the gate is present turns on the 'carriage skip interrupt' FF. Thus, sensing any carriage tape hole causes a 'printer level 1 interrupt request.'

The carriage skip interrupt (skip response) position of the DSW is set to a 1, and a 1 is also present to indicate the channel in which a hole was sensed. The program analyzes the DSW to determine whether or not the skip operation should be ended. In any case, 'XIO sense reset 15' and 'B bit 1' are required to turn off the 'carriage skip interrupt' FF. When the skip is to be ended, the program gives an 'XIO control' instruction with the modifier bit 14 set to 1.

'Printer control load' and 'U reg 14' turn on the 'skip stop latch.' The next time 'carriage CB' is activated, the 'skip start latch' turns off. 'Carriage magnet select' and 'interposer magnet select' are both deactivated, and the skip operation terminates.

As long as either 'interposer magnet select' or 'carriage magnet select' is active, the 'printer DSW bit 3' line is also active. This line sets a 1 in the bit 3 position during a sense DSW operation, indicating that the carriage is busy.

Space

- Modifier bit 15 = 1 causes the programmed space control function.
- Space turns on the 'line space' latch.
- Forms are advanced one space.
- Operation is stopped by the first CB pulse.
- Level 1 interrupt is requested at the end of the operation.
- Maintenance Diagram XP511.

'Printer control load' and 'U reg 15' turn on the 'line space' latch, activating 'carriage magnet select' to the 1132. Forms movement starts when the carriage clutch engages. The 'interposer magnet select' line is not activated for a space operation. Activating the 'carriage CB' line turns off the 'line space' latch. The clutch disengages, and forms movement stops after one line space without need for another instruction.

Figure 1-7 shows in simplified form the circuit to turn on the 'carriage space interrupt' FF at the end of the space operation. The flip-flop turns on at the end of a phase B pulse after the 'line space' latch turns off.

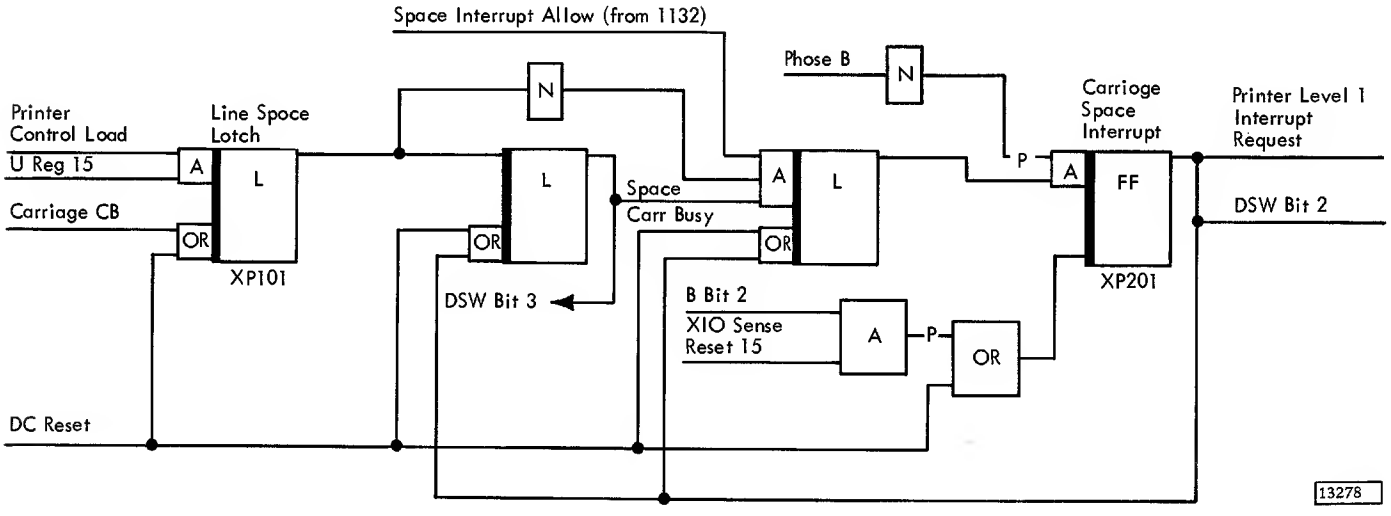
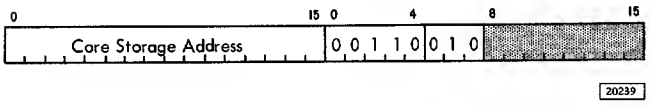


Figure 1-7. Carriage Space Interrupt

READ (010)

- The read function code causes a read emitter operation.
- The XIO instruction appears in the interrupt level 1 servicing subroutine.
- Read emitter is programmed if the last previous level 1 interrupt request resulted from a read emitter response. However, read emitter is not programmed if the last character for a line of print has been scanned.
- Read emitter gates the character from the 1132 printer emitter to the I/O bus. From there the character is set into storage.
- Maintenance diagram XP501.

When the function code in the IOCC for an XIO instruction is 010 (read), a read emitter operation occurs. The IOCC for this function is:



The program must determine whether the read emitter operation is required. If all characters for a line of print have been scanned and the print magnets energized, the emitter need not be read again until the next print operation is started.

During the E3 cycle in the CPU, the 'XIO read' and 'area 6' lines are activated and condition two inputs each to eight AND's in the adapter. Each of the 'print disk bit 0' through 'print disk bit 7' lines from the printer can complete the conditioning of an AND. The corresponding 'printer data bit 0' through 'printer data bit 7' lines then become active. The standard E3 functions in the CPU then store the bits in positions 0 through 7 of the addressed core storage word.

Once the emitter character is set into core storage, the program can start comparison with the print data table. Setting of the new printer scan field starts in preparation for printing the character read from the emitter.

MANUAL OPERATIONS

- Adapter circuits accept signals from the 1132 and return signals to the 1132, thus controlling mechanical operations of the 1132.
- Operating keys on the 1132 initiate these operations.

Printer Start Key

- Pressing the printer start key is necessary to prepare for programmed printer operations.
- Maintenance Diagram XP501.

Pressing the 1132 start key turns off the 'stop' latch if the 'stop' latch has previously been turned on by pressing the stop key. In addition, the 'ready' latch is turned on if none of these conditions is blocking the turn-on:

1. Motor switch is off.
2. Stop key is being pressed while 'run' latch is on.
3. Coincidence of 'printer stop' line active and either 'forms contact' or 'stop latch' active.

These same conditions can turn off the 'ready' latch if it is on.

The 'printer stop' line, previously referred to, can be activated by:

1. Stop printer XIO control instruction.
2. 'CPU stop' latch active.
3. 'Printer dc reset' active.

Activating 'printer stop' turns off the 'ready' latch, only when there are no forms in the printer or the stop key has turned on the 'stop' latch.

Printer Stop Key

- Pressing the printer stop key removes the printer from the ready status.
- Maintenance Diagram XP501.

Pressing the stop key while the 'run'latch is off turns off the 'ready' latch and turns on the 'stop' latch. However, if the 'run' latch is on, pressing the stop key only turns on the 'stop' latch. Later, when 'printer stop' turns off the 'run' latch, 'printer stop' and the fact that the 'stop' latch is on turns off the 'ready' latch.

Carriage Space Key

- Pressing the carriage space key results in moving the forms one line space.

- No interrupt request occurs at the end of the manual space operation.

- Maintenance Diagram XP511.

Pressing the space key when the 'printer run' latch is off turns on the 'manual space' latch, activating the 'carriage magnet select' line. The carriage clutch engages and the forms movement starts. The first 'carriage CB' pulse from the 1132 turns off the 'manual space' latch, and the forms move only one line space.

No interrupt request results from a manual space operation. The manual space operation does, however, turn off the 'use meter' latch if it is on.

Carriage Restore Key

- Pressing the carriage restore key causes the forms to move until carriage brush 1 is read.

- Unlike other skip operations, no interrupt requests occur when holes are sensed in the control tape.

- Maintenance Diagram XP511.

When the 'printer run' latch is off, pressing the restore key turns on both the 'restore' latch and the 'skip start' latch. The operation proceeds like a programmed skip except that the 'restore' latch being on prevents 'any carriage channel' from turning on the 'carriage skip interrupt' FF.

The 'restore' latch being on allows 'carriage brush 1' to turn on the 'skip stop' latch. 'Skip stop' latch and the next available carriage CB pulse turn off the 'skip start' latch and the 'restore' latch. Deactivating 'carriage magnet select' then turns off the 'skip stop' latch.

Carriage Stop Key

- Pressing the carriage stop key stops any forms movement that is taking place.

- Maintenance Diagram XP511.

Pressing the carriage stop key while the 'carriage magnet select' line is active turns on the 'skip stop' latch. The 'skip stop' latch cannot latch unless 'carriage magnet select' is active (forms are feeding). The next available carriage CB pulse turns off the 'skip start' latch. Also turned off, if it is on, is the 'restore' latch.

If the key is pressed while a programmed skip is taking place, another start carriage function must be provided by the program. There is no other way to resume the skip.

If the key is pressed during a restore operation, stopping occurs at the next CB time. The restore operation can be resumed by pressing the restore key again.

USE METER (1132)

- Printer adapter circuits provide the 'use meter select' line to the 1132 use meter.

- Maintenance Diagram XP511.

The 'printer run latch' line being active turns on the 'use meter' latch, provided neither the 'manual space' latch nor the 'restore' latch is on. Should either of these latches be on, the 'use meter latch' does not turn on until the one that is on turns off. While the 'use meter' latch is on, 'use meter select' is active any time that the 'CPU run' line is active.

After 'printer run latch' is deactivated, the 'use meter' latch remains on. Turning on either the 'manual space' latch or the 'restore' latch at this time turns off the 'use meter' latch.

FEATURES

There are no features available for the IBM 1132 Printer adapter.

POWER SUPPLIES AND CONTROL

Power for the IBM 1132 Printer adapter is provided and controlled by the CPU.

CONSOLE AND MAINTENANCE FEATURES

There are no console and maintenance features in the IBM 1132 Printer Adapter. Functions of the operator panel keys on the 1132 printer are described in "Manual Operations," in Part 1 of this manual.

INTRODUCTION

FUNCTIONS OF THE IBM 1442 CARD READ PUNCH

- Three models of the 1442 (Model 5, 6, and 7) are available.
- Models 6 and 7 provide card input to the system.
- Models 5, 6, and 7 provide card output from the system.
- Maximum Speeds

	Reading	Punching
Model 5:	None	160 columns per second
Model 6:	300 cards per minute	80 columns per second
Model 7:	400 cards per minute	160 columns per second

- Models 6 and 7 provide for loading of programs if no IBM 2501 Card Reader is installed.
- For additional information on the 1442 unit, refer to the IBM Field Engineering Theory of Operation, 1442 Card Read Punch, Models 5, 6, and 7, Form Y31-0101.

Models 6 and 7 of the 1442 provide both input and output for the IBM 1130 Computing System. These models can also provide a program load function when the program load key is pressed. This input operation is in addition to program controlled reading operations. If, however, the system contains an IBM 2501 Card Reader in addition to the 1442 model 6 or 7, the program load function is performed by the 2501. Program loading from an IBM 1134 Paper Tape Reader is not possible when a model 6 or 7 is included in the 1130 system.

Model 5 of the 1442 provides punched card output only from the system and has the same punching characteristics as the model 7. A system cannot include both a model 5 and a model 6 or 7. The model 5 has the further limitation that it cannot be used with an 1131 CPU that operates on 115 volts.

The 1442 is a single unit (Figure 2-1) that processes cards serially, column by column, from a single supply hopper. All cards first pass the read station (models 6 and 7), then the punch station. This permits each card to be read, punched, or read and punched. Reading and punching cannot occur simultaneously (that is, one card cannot be punched while the following card is being read) because the reading and punching rates are different. Data flow and control are shown in XR401.

ADAPTER CONTROLS

- Punching or reading operations are under direct program control of the CPU.
- The area code for the 1442 is decimal 2 (binary 00010).
- Control lines from the CPU to the adapter define the operation to be performed by the 1442 and provide timings.
- Control lines from the adapter to the CPU signal that an interrupt is requested.

When the CPU executes an XIO instruction, decoding of the control word of the IOCC activates control lines to all I/O adapters. An area code of 2 (00010) causes these lines to affect the adapter circuits for the 1442. The control lines that are applicable to the 1442 adapter are:

1. 'XIO sense interrupt.
2. 'XIO sense device.'
3. 'XIO control.'
4. 'XIO write.'
5. 'XIO read.'
6. 'XIO sense reset 15.'

Decoding of modifier bits of the IOCC while present in the U-register further defines the operation to be performed by the 1442.

The 'program load to SRP' line is activated when the CPU program load key is pressed. The result is the loading of information from one card into 80 core storage locations, starting in location /0000, accomplished without need for an instruction.

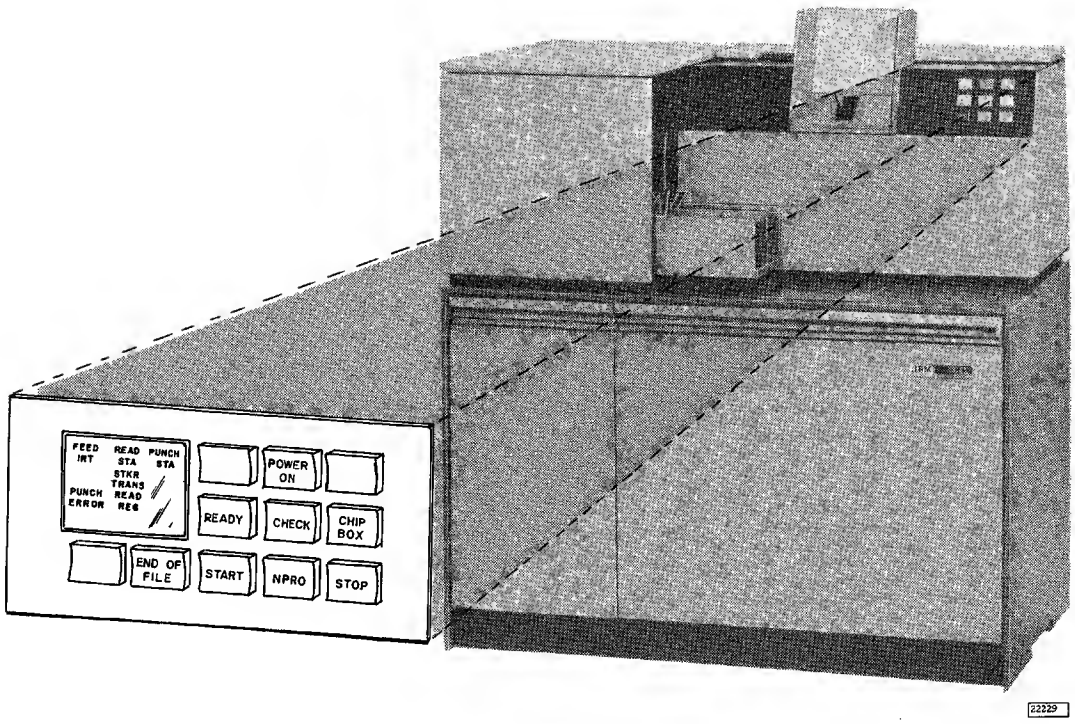


Figure 2-1. 1442 Card Read Punch

Control lines are also activated to provide CPU timing pulses to the adapter circuits and to indicate certain conditions within the CPU.

Control lines from the adapter to the CPU signal conditions in the adapter. Activating either 'level 0 response' or 'level 4 response' results in an interrupt request in CPU circuits. Also a control line to the CPU is activated to indicate that the 1442 is ready to perform an operation.

Control and signal lines to and from the 1442 affect the operation of the adapter. Conversely, adapter circuits affect the 1442 operation. Figure 2-2 shows components of the 1442 which affect or are affected by the adapter.

PUNCH OPERATION

- Usual programming procedure checks that the 1442 is ready before starting a punch operation.
- Punch operation is started by a control function code and a start punch modifier in the IOCC. Intermittent card motion through the punch station starts.

Lights	Switches	CB's	Magnets Relays and Miscellaneaus
Read Reg	Transpart	Feed CB 1	Incremental Drive Magnet A
Punch	Start	Feed CB 2	Incremental Drive Magnet B
Power On	Nan Pracess Runaut	Feed CB 3	Stacker Select Magnet
Ready	Stap	Feed CB 4	12 Punch Magnets
Feed Clutch	Happer Empty	Punch CB 1	Matar Relay
Check	Stacker Jam	Punch CB 2	Clutch Relay
Happer	Idle Relay Contact	Incremental Drive CB A	15 Secand Delay Relay
Punch Station		Incremental Drive CB B	Pracess Meter
Read Statian			Read Phatacells
			Read Emitter

22230A

Figure 2-2. 1442 Circuit Campanents

- Punching mechanism provides timing pulse for each column to cause punch response interrupt request (level 0).
- Data is transferred by a write function code in the IOCC.
- Checking of previous column punched occurs just prior to transferring data for new column.
- Data word for the last column to be punched must contain a 1 in the bit 12 position.
- An operation complete interrupt request (level 4) occurs at the end of punching.
- Only one group of columns can be punched per card. Punching cannot be restarted after the operation complete interrupt.

Before the instruction to start a punching operation, the program usually includes a sense device instruction to determine whether or not the 1442 is ready. The same instruction allows a test for a 1442 busy condition. If the 1442 is ready and not busy, the program issues an XIO instruction with an IOCC containing the control function code and start punch modifier.

If a card is entering the punch station, the incremental punch drive causes the card to start moving through the punch station (Figure 2-3). Otherwise the feed clutch is energized and a card is fed into that position. Then the incremental punch drive starts moving the card.

A punch CB provides the timing pulse to start the checking of the previous column punched. Before column 1 has been punched, this check has no significance. However, just before the data for column 2 is transferred to the adapter, column 1 punching can be checked. Signals are generated for each position (12, 11, 0,...,9) that was punched in column 1. These signals are compared with the contents of a register (data register) containing the data transferred for column 1. Any difference indicates a punch error in column 1. The process of checking the previous punching just before interrupting for a new data transfer continues throughout the punching operation.

Another timing pulse, following the checking process, causes a punch response interrupt request (level 0). The CPU program, in servicing the interrupt, issues an XIO instruction with the IOCC containing a write function code. Execution of this instruction loads the data register with data from the B-register. B-register bit 0 position sets data register 12, which controls punching in the 12 row of the card. Figure 2-4 shows the standard data transfer paths. The program must provide properly coded data for punching.

The procedure of checking the previous punch, interrupting, and loading the data register is repeated for each column. The punching operation stops when the word being loaded into the data register contains a 1 in the bit 12 position. After the punching in the last punched column is checked, the 1442 is no longer busy. An end operation response (level 4) results in an interrupt request to the CPU. Once punching has terminated, it cannot be restarted in the same card. An attempt to do so feeds another card.

READ OPERATION

- Usual programming procedure is to check that the 1442 is ready before starting a read operation.
- Read operation is started by a control function code and a start read modifier in the IOCC. Read feed starts.
- For each column, the reading mechanism provides timing pulses that cause setting the data register with data read from the card.
- Setting of the data register is checked by reading punched holes again.
- For each column, after the data register is set, a timing pulse causes a read response interrupt request (level 0).
- XIO instruction with a read function code in the IOCC causes transfer of data to CPU core storage for each column.
- After column 80 has been read, an end operation interrupt request (level 4) occurs.

Before the instruction to start a read operation, the program usually includes a sense device instruction to determine whether or not the 1442 is ready. The same instruction allows a test for a 1442 busy condition. If the machine is ready, a card is in position to start past the reading photocells during the next feed cycle.

Reading is started by an XIO instruction with an IOCC containing the control function code. The modifier specifies start read. Execution of the instruction

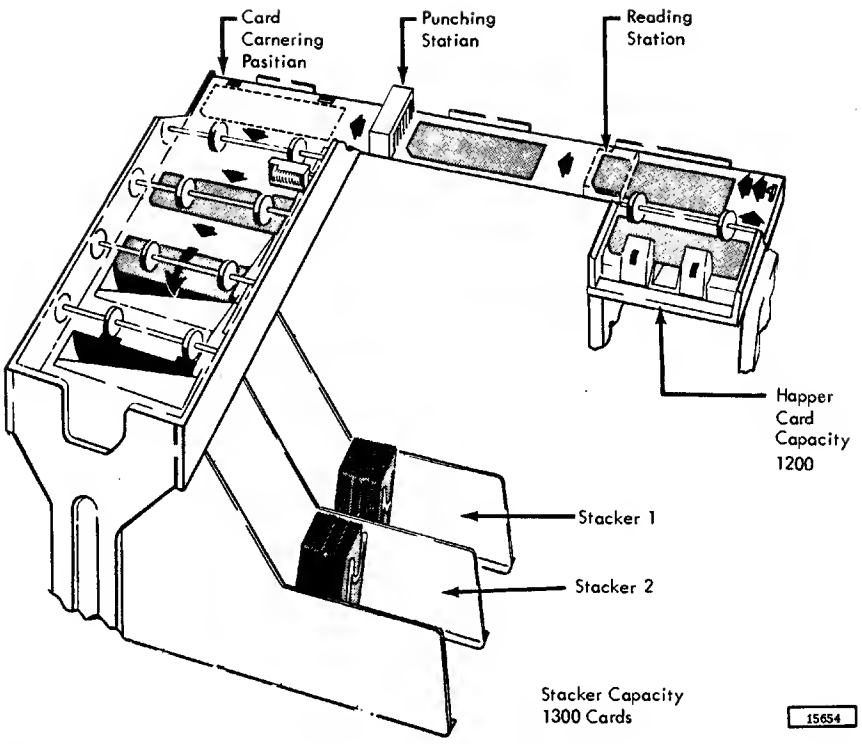


Figure 2-3. Card Feed Path

causes a card feed cycle to start and sets the adapter circuits to read a card. Card motion is continuous and does not stop until the card is registered in the punching station.

The card is read serially -- that is, column by column -- beginning with column 1. Reading is accomplished through the principle of photocell sensing. Figure 2-5 illustrates the path of the card through the photocell reading mechanism. While each card column is read by the photocells, the output is sampled twice and the readings are compared for agreement. A third sample pulse then sets the data register.

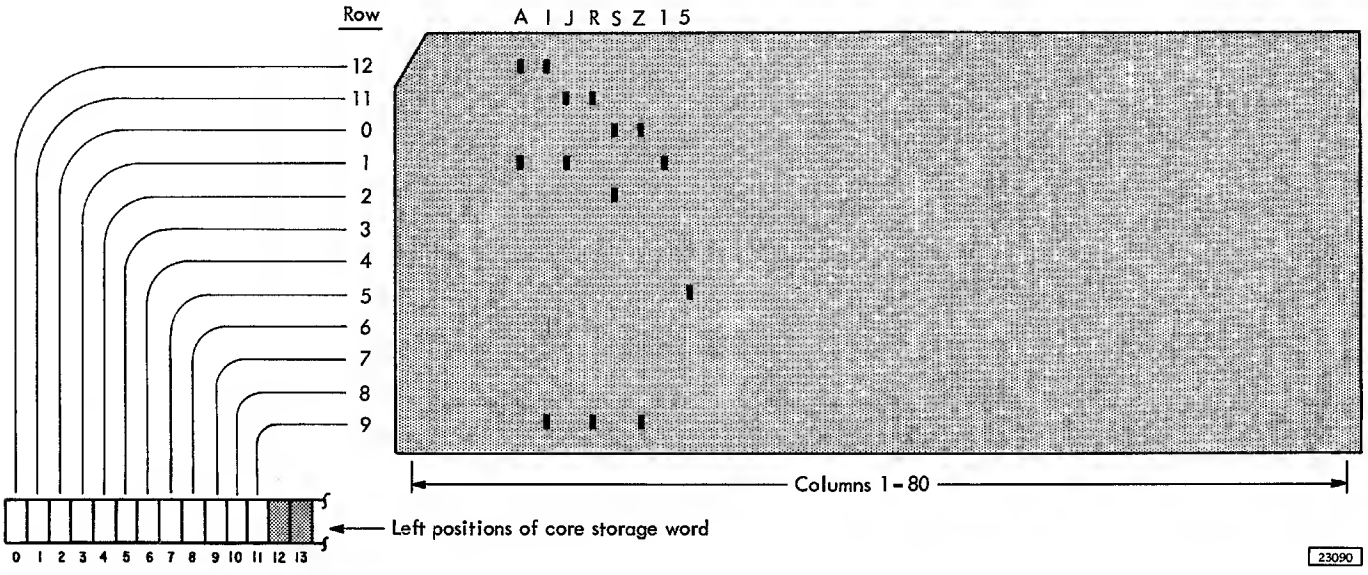


Figure 2-4. Data Transfer Paths

After the data register has been finally set for each column, a timing pulse causes a read response interrupt request (level 0). The interrupt servicing subroutine includes an XIO instruction with an IOCC containing the read function code. Execution of this instruction transfers the contents of the data register to CPU core storage, via the B-register.

The read-check-read process followed by an interrupt request occurs for each column until all 80 columns have been read. A timing pulse, after column 80 has been read, terminates the read operation and the 1442 busy condition. Then an end operation response causes a level 4 interrupt request in the CPU.

PROGRAM LOAD OPERATION

- Operation is accomplished by the 1442 if no 2501 is also included in the system.
- Pressing the CPU program load key starts the operation.
- Data from each column is loaded into a core storage location, starting at /0000 and progressing to /004F.
- After reading one card, CPU uses the contents of location /0000 as the first instruction and starts execution of that instruction.

On systems without an IBM 2501 but including an IBM 1442, model 6 or 7, the program load operation is performed by the 1442 under control of the adapter. After a system reset and the run in cycle of a load card (making the 1442 ready), program load can be initiated by pressing the program load key on the 1130 console. This load mode operation causes the load card data to be placed in 80 consecutive memory positions beginning at memory location /0000. The data paths are different from a programmed read operation (Figure 2-6).

After reading the load card, the operation forces a CPU cycle. This cycle is an I1 cycle and the core storage address used is /0000 (IAR was reset). Thus execution starts with the instruction in column 1 of the load card.

SELECTIVE STACKER OPERATION

- Cards normally are stacked in stacker 1.
- An XIO instruction with an IOCC containing a control function code and stacker select

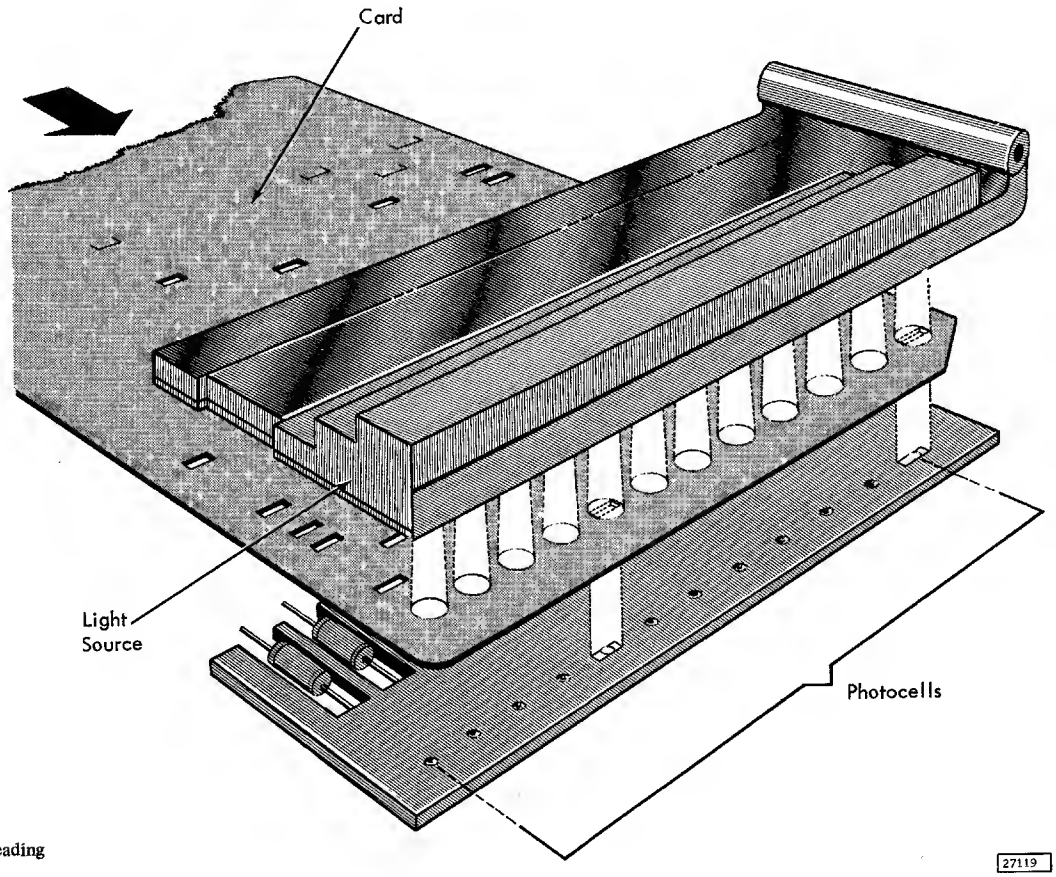


Figure 2-5. Photocell Reading

modifier causes stacker selection. The card is stacked in stacker 2.

FEED CYCLE OPERATION

- An XIO instruction with an IOCC containing the control function and the feed cycle modifier starts this operation.
- Execution of the instruction advances all cards in the feed into the next station.
- No reading or punching takes place.
- Read responses do not occur.
- When feeding is complete, an end operation response causes a level 4 interrupt request in the CPU.

LAST-CARD SEQUENCE

- Last-card condition can be recognized by the program (sets a 1 in the DSW).
- Operator determines what further action is required.
- Adding cards in hopper and pressing start key cause continued processing.
- Pressing start key without adding cards starts the last-card sequence.
- Last-card sequence causes two feed cycles to process and stack the last card, terminating operations.

While the hopper becomes empty during a feed cycle, a last-card condition is recognized. This condition removes the 1442 ready status and sets the not ready indicator in the device status word. The operator may continue processing cards by loading more cards into the hopper and pressing the start key or he may initiate a last-card sequence by pressing the start key without loading more cards in the hopper.

When the start key is pressed without cards in the hopper, the 1442 is placed in the ready condition and allows two more feed cycles to be taken.

PROGRAMMING NOTES

- Reading a card also feeds the preceding card through the punching station if it has not already been moved by a previous feed or punch operation.
- Correct programming is required to obtain maximum operating speeds.

The 'start read' instruction causes a card at the punch station to be transported through the punch station to the stacker. The card being read moves from the preread station to the punch station as the

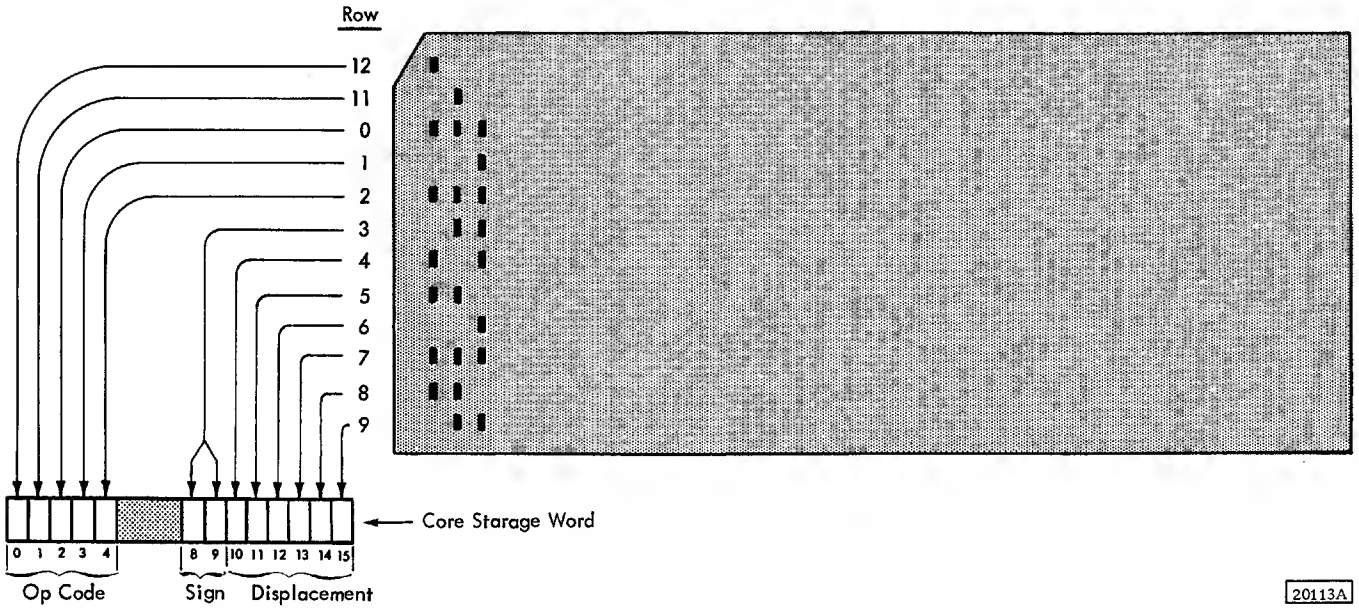


Figure 2-6. Program Load Data Transfer

following card feeds from the hopper to the read station.

Maximum reading rates are attained only when successive start read commands arrive early enough to reenergize the read clutch before the clutch latch point is reached. To accomplish this, successive 'start read' commands must arrive within 35 milliseconds, model 6, or 25 milliseconds, model 7, after the operation complete interrupt from the previous read operation. If a 'start read' command does not arrive within this time, the maximum reading rate becomes 285 cards per minute for model 6 and 375 cards per minute for model 7.

When data from less than 80 columns of the card is to be stored, CPU processing time can be saved. The servicing subroutine for read responses from columns that are not to be stored can be shortened. This programming makes more time available for computing.

Punching rates depend on the position of the card when the last column has been spaced or punched. The punching speed ranges are:

Model 6 -- 49 cpm to 262 cpm.
Model 5 and 7 -- 91 cpm to 355 cpm.

The approximate time required to process a single card is:

Model 6 -- 216 ms + 12.5 ms per card column spaced or punched.
Model 5 and 7 -- 163 ms + 6.25 ms per card column spaced or punched.

Figure 2-7 shows the approximate punch cycle times and cards-per-minute rates based upon the last column punched.

It is important to consider card design when the operation calls for reading a card, processing the information, then punching the results into the same card. A significant increase in card throughput results from punching into the beginning columns of the card.

Last Column Punched	Punch Time (ms)		Total Punch Cycle Time (ms)		Cards per Minute	
	Model 6	Model 5&7	Model 6	Model 5&7	Model 6	Model 5&7
1	13	6	229	169	262	355
10	125	63	341	226	176	265
20	250	125	466	288	127	208
30	375	188	591	351	102	171
40	500	250	716	413	84	145
50	625	313	841	476	71	126
60	750	375	966	538	62	112
70	875	438	1091	601	55	100
80	1000	500	1216	663	49	91

30129

Figure 2-7. Punch Cycle Times and Rates

FUNCTIONAL UNITS

BUFFER REGISTER

- The 1442 serial read punch (SRP) unit uses a buffer register (also called data register) in the adapter for data transfer and data checking.
- SRP buffer register contains 12 flip-flops. Each FF corresponds to a punching row of the card.
- Register is loaded from the B-register with data for punching.
- Register is set from reading holes in the card during a reading operation.
- Checking of either punch or read data uses the SRP data register (DR) latches.

Transfer of data to be punched occurs during a CPU E3 cycle resulting from an XIO instruction with a write function code and area 2. At T4, with 'SRP ready' and 'SRP punch SS gate' active, the 'load punch data' line becomes active. The voltage shift occurring when 'load punch data' is activated causes the 'load punch data sample pulse (SP)' to be activated. The sample pulse then turns on any 'SRP data register' flip-flop that is gated by the corresponding B-register flip-flop being on.

At the end of the T4 that loads the register, the 'punch data trigger' FF turns on. Then the outputs of the register flip-flops are gated to the 'punch magnet' lines that go to the 1442 device circuits.

While the 'SRP read' line is active in a read operation, each hole that is sensed by a solar cell activates the corresponding 'register complement bit' line. The 'register complement bit' lines gate both the turn-on and turn-off of the data register flip-flops. Thus, when the 'register complement SP' is activated, the state of any flip-flop is changed if the corresponding hole in the card is being sensed. The final setting of the data register determines the data that is transferred to the CPU core storage.

The turning on, turning off, and complementing of the data register flip-flops should result in all of them being off at the time of the error sample. In a punch operation, the 'punch interrupt and error SP'

occurs when the 'time 2' FF turns off. In a read operation, the 'read interrupt and error SP' occurs when the 'time 2' FF turns off the second time (after the SRP read SS times out).

PRINCIPLES OF OPERATION

- The 1442 adapter initiates action by the 1442 as the result of an XIO instruction in the CPU program.
- The area code for the 1442 is decimal 2 (00010).
- Function codes that are applicable to the 1442 are:

  Sense interrupt.
  Sense device.
  Control.
  Write.
  Read.

- The adapter also controls a program load operation that results from pressing the CPU program load key.

SENSE INTERRUPT (011)

- Sense interrupt sets an interrupt level status word (ILSW) in the accumulator of the CPU.
- Area code is not required.
- ILSW is set for the highest level of interrupt active when the instruction is given.
- 1442 interrupts on level 0 or level 4.

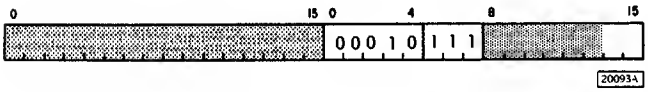
An XIO instruction with a function code of sense interrupt activates the 'XIO sense ILSW' line from the CPU. If 'interrupt level 4' is active when the instruction is given, the 'end operation response' activates 'ILSW bit 2'. Bit 2 in the ILSW indicates that the 1442 requested an interrupt at the end of an operation.

The 1442 is the only device that interrupts on level 0. Therefore, no sense interrupt is required in servicing a level 0 interrupt request.

SENSE DEVICE (111)

- Sense device sets the device status word (DSW) in the accumulator of the CPU.
- Status conditions in the 1442 result in 1's being set in the DSW during the CPU E2 cycle.

An XIO instruction with a sense device function code in the IOCC causes the DSW to be set in the CPU accumulator during the E2 cycle. The IOCC is:



The DSW for the 1442 is shown in Figure 2-8. Three conditions cause interrupt requests on level 0 or level 4 as shown.

Significance of DSW Bits

Read Response (Models 6 or 7): A 1 in position 0 indicates the 'read response trigger' FF has been turned on. A column of data is ready to be transferred to the CPU core storage. The level 0 interrupt request that results must be serviced within 800 microseconds for the model 6 and within 700 microseconds for the model 7.

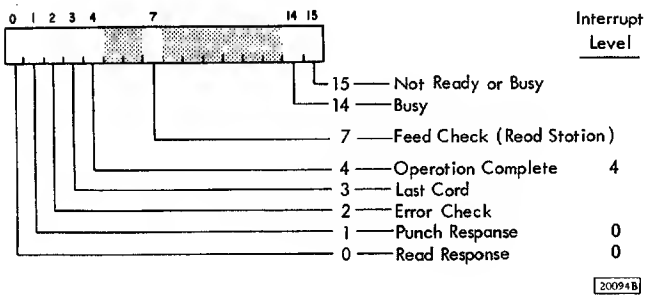


Figure 2-8. Device Status Word (1442)

Punch Response: A 1 in position 1 indicates that the 'punch response trigger' FF has been turned on. The level 0 interrupt request that results must be serviced by transferring a column of data from the CPU within approximately 300 microseconds.

Error Check: A 1 in position 2 indicates one or more of these conditions are true, activating 'SRP error' and lighting the 1442 check light.

1. The 'feed clutch latch' is not on when 'feed CB1' is activated. The feed clutch light on the 1442 lights.
2. 'Data error' is active because either the 'read error trigger' or the 'punch error trigger' has been turned on. The read error or punch error light on the 1442 also lights.
3. 'Parity stop' line from the CPU is active, because a character from core storage has read or written with incorrect parity.
4. The 'misfeed' latch is on, and 'feed CB3' is active. This condition occurs when there are cards in the 1442 hopper, but a feed cycle fails to feed a card to the read station. The hopper light on the 1442 lights.
5. The 'feed check punch station' latch is on. This condition occurs when 'feed CB3' is activated while 'punch lamp dark' is active. The punch station light on the 1442 lights.
6. The 'feed check punch station' latch is on. This condition occurs when 'feed CB2' is activated while 'any lamp dark' is active. The read station light on the 1442 lights.
7. The 'stacker jam' latch is on, because the stacker jam switch has been transferred. The transport light on the 1442 lights.

Last Card: A 1 in position 3 indicates that the 'last card trigger' FF is on. When the operator presses the start key after the hopper is empty, the last card starts through the read station. When 'feed CB 1-2' is activated the 'last card trigger' turns on. It stays on until the following card feed cycle, when 'feed CB 1-2' becomes active again. Turning off 'last card trigger' turns on the 'block SRP end op trigger'.

Operation Complete: A 1 in position 4 indicates the 'end operation response' is active, because the 'end operation' FF has been turned on.

Feed Check (Read Station): A 1 in position 7 indicates that the 'feed check read station' latch is on. This status condition also sets the error check bit (bit 2 position) and lights the read station light on the 1442.

Busy: A 1 in position 14 indicates that one of these lines is active:

1. 'Punch SRP.' This line is active when either 'incremental drive A trigger' or 'incremental drive B trigger' is on.
2. 'SRP XIO punch.' This line is active when the 'XIO punch trigger' is on.
3. 'SRP feed or program load'. This line is active when the 'XIO feed trigger' is on, or when the 'program load' line from the CPU is active.

The same instruction that turns on the 'XIO read trigger' also turns on the 'XIO feed trigger.' Thus, one of the lines previously described is always active during any program load, read, punch or feed operation.

The busy condition also sets a 1 in position 15 of the DSW.

Not Ready or Busy: A 1 in position 15 indicates the 'ready latch' is off or the 1442 is busy. The conditions which make the 1442 busy have been described previously. Busy sets 1's in both positions 14 and 15 of the DSW.

When position 15 only contains a 1, the not ready condition is indicated. Either the 'ready latch' has never been turned on or has been turned off after being turned on. To turn on the ready latch it is only necessary that a card move into the read station during a cycle in which the 'start latch' is on.

The 'ready' latch is turned off, setting the 1 in DSW position 15 when:

1. The 'stop' latch is turned on and the 1442 is not busy. The 'stop' latch is turned on by pressing the stop key.
2. A power on reset occurs or the 'nonprocess runout (NPRO)' latch is turned on. The 'NPRO' latch is turned on by pressing the NPRO key on the 1442 when the 1442 is not busy.
3. An SRP error occurs.
4. The hopper becomes empty, unless the card in the read station is the last card.

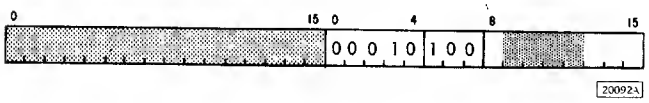
Sense Reset

Modifier bit 15 = 1 turns off the responses that cause level 0 interrupt requests. These are read response and punch response. Modifier bit 14 turns off the end operation response that causes a level 4 interrupt request.

CONTROL (100)

- Control function code causes the 1442 to perform the operation specified by the modifier bits 8, 13, 14, or 15.
- Modifier 8 causes one card to enter stacker 2.
- Modifier 14 causes all cards in the feed to advance one station.
- Modifier 15 causes the start of a punch operation and sets the adapter to activate interrupt requests on signal from the 1442.
- Modifier 13 causes the start of a read operation and sets the adapter to activate interrupt requests on signal from the 1442.
- Maintenance Diagram XR501, XR511.

During the E2 cycle of the CPU, 'area 2' and 'XIO control' lines to the adapter are activated. If the 1442 is ready and not busy, the adapter 'area 2 control' line becomes active. The 'area 2 control' line gates the turn-on of adapter latches along with modifier bits decoded in the CPU U-register. The IOCC is:



The function caused by each modifier bit is:

Bit 8 -- 'Stacker select'
Bit 14 -- 'Feed cycle'
Bit 15 -- 'Start punch'
Bit 13 -- 'Start read'

Only one modifier bit position should be set to 1, because only one operation can be performed by each XIO instruction.

Stacker Select (Models 6 and 7)

- Modifier bit 8 specifies the stacker select operation.
- Stacker select causes the card leaving the punch station to enter the alternate stacker (stacker 2).

'Area 2 control' and 'U-register 8' gate the 'XIO stacker trigger' so that a T4 pulse from the CPU can turn it on. With the 'XIO stacker trigger' on, the end of the next 'feed CB 1-2' pulse turns on the 'stacker select trigger' and turns off the 'XIO stacker trigger.' The 'stacker select trigger' being on energizes the stacker select magnet until feed CB 1-2 makes again (CB1 time). The feed CB timing is needed because the selection is made after punching but before the card reaches the stacker.

Feed Cycle

- Modifier bit 14 causes a feed cycle operation.
- Feed cycle causes all cards in the feed path to advance to the next station.
- Feed cycle operation causes end operation response (operation complete) interrupt request.

'Area 2 control' and 'U-register 14' gate the 'XIO feed trigger' so that a T4 pulse from the CPU can turn it on. The 'XIO feed trigger' being on turns on the 'feed clutch' latch provided 'SRP motor delay' is active and 'SRP feed interlock' is not active. The 'feed clutch' latch being on activates the line to energize the 1442 feed clutch magnet.

If the 'SRP motor delay' line is not active, the 'motor' latch must be turned on and 'delay' must be activated. Turning on the 'XIO feed trigger' activates the 'SRP busy' line, which can turn on the 'motor' latch. 'SRP motor' activates 'delay' after approximately 850 ms.

Energizing the feed clutch starts a feed cycle which advances all cards in the feed. When the 'XIO feed trigger' turns off at the end of 'feed CB 1-2', the 'SRP busy' line is deactivated. The 'end operation' FF turns on unless the 'block SRP end op trigger' is on. The latter trigger is only turned on in a last-card sequence.

Start Punch

- Modifier bit 15 causes a start punch operation.
- Start punch causes a feed cycle if there is no card in position to start punching.
- With card in position, start punch starts incremental drive motion.

- Start punch sets the adapter so that punch response interrupt requests occur for each column.

- Maintenance Diagrams XR501, XR701.

'Area 2 control' and 'U-register 15' activate the 'SRP set XIO punch' line, gating the turn-on of the 'XIO punch trigger.' A T4 pulse then turns on the 'XIO punch trigger.' The end of activation of the 'SRP set XIO punch' line causes a 'register reset SP (sample pulse).'

The 'XIO punch trigger' remains on until the end of 'punch CB 1-2' time of the last column to be punched. In order to activate 'SRP start punch' there must be a card in the punch station, no feed interlock, and the 1442 must be ready with the motor running. Manual intervention is required if the 1442 is not ready. If the 1442 is ready, but there is no card in the punch station, the adapter starts the motor and engages the feed clutch.

Turning on the 'XIO punch trigger' activates 'SRP busy,' which can turn on the 'motor' latch. After approximately 850 ms, 'SRP motor' activates 'delay.' At that time 'motor delay' becomes active, and the 'feed clutch' latch can turn on, provided that 'feed interlock' is not active. During the feed cycle, 'feed interlock' is activated from the start of 'feed CB 1-2' until 'feed CB4' turns off the latch.

In review, start punch has ensured that there is a card in position to punch, has turned on the 'XIO punch trigger,' and has activated the 'SRP start punch' line.

Checking Previous Column

- 'XIO punch trigger' FF is on and the 'SRP start punch' line active from start punch operation.

- Punch gate singleshot starting to time out starts the time 1-time 2 sequence.

- Time 2 causes punch magnet echo impulses to turn off all data register FF's representing punches in the previous column.

- End of time 2 checks for any data register FF being on. Any one being on allows turning on the 'punch error trigger.'

- End of time 2 also turns on the 'punch response trigger,' setting a 1 in DSW position 1 and activating level 0 interrupt request in the CPU.

- Subroutine instruction execution reloads the data (buffer) register. (See "Write.")

The 'SRP start punch' line allows the turning on of the 'incremental drive latch,' by an 'incremental drive CB A' pulse, to turn on the 'incremental drive A trigger' FF. The latter FF activates the 'punch SRP' line so that the next punch CB 1 can start the punch gate singleshot (SS). The start of the active SS output turns on the 'time 1' FF.

The 'time 1' FF stays on until the 'oscillator A (frequency divider)' FF turns on. (The length of time that 'time 1' is on varies because the turn-on has no relationship to the CPU oscillator.) Turning off 'time 1' turns on the 'time 2' FF. Turning on the 'time 2' FF fires the register complement sample pulse drivers (SPD's). At this same time the 'punch echo 0-9, 11, 12' lines from the 1442 are active for each hole punched in the previous column. (In the adapter, these lines are called the 'punch check amplifier 0-9, 11, 12' lines.) The still active 'punch SRP' line ANDs with the punch check amplifier lines to activate the corresponding 'register complement bit 0-9, 11, 12' lines.

Each register complement bit line that is active means that position was punched in the previous column. An active register complement bit line allows the register complement sample pulse to change the state of the corresponding data register FF. The data register FF's that are on still represent the data which should have punched in the previous column. Thus, only the data register FF's that are on should have their status changed (be complemented). Any FF left on or turned on indicates a punch error.

The 'time 2' FF is turned off by the second 'oscillator A' following the pulse that turned off 'time 1.' Turning off 'time 2' fires an SPD and activates 'punch interrupt and error'. This sample pulse can turn on the 'punch error trigger' if any data register FF is on. The same sample pulse turns on the 'punch response trigger.' The 'punch response' line then gates the setting of DSW bit 1, and the 'level 0 response' line is activated to the CPU.

The instruction in the level 0 servicing subroutine to reload the data register must be given while 'SRP punch SS gate' is still active. Otherwise the 'load punch data' line cannot be activated, and data is lost. Data transfer is described under the heading "Write." Activating the 'XIO sense reset 15' during the subroutine is required to turn off the 'punch response trigger.'

When the holes have been punched, the incremental drive mechanism moves the card to the next column. When two or more columns are punched in a card, both 'incremental drive A trigger' and 'incremental drive B trigger' are turned on. Then they remain on until the punch gate SS times out after punching the last column.

Punching and Checking the Last Column

- Data word for the last column to be punched must contain a 1 in bit position 12 in addition to the data.
- Bit 12 is sensed during data transfer in a write operation.
- If all 80 columns are to be punched the bit 12 must be in the 80th data word transferred.
- No punch response occurs after the last column has punched and been checked.
- End operation response causes a level 4 interrupt request.
- A feed cycle is required before another punch operation can start.

When the data word for the last column to be punched is set in the data register by a 'load punch data SP,' the 'B bit 12' allows the sample pulse to turn on the 'last punch trigger.' Then 'punch CB 1-2 latch' turning off turns off the 'XIO punch trigger.' The fact that 'SRP XIO punch' is no longer active prevents the turn-on of the 'punch response trigger.'

Timing out of the punch gate SS turns off both the 'incremental drive A' latch and the 'incremental drive B' latch. The turn-off of these latches has been gated since 'SRP start punch' was deactivated by turning off the 'XIO punch trigger.' With both the incremental drive latches off, 'punch SRP' is deactivated.

When both the 'SRP XIO punch' and 'punch SRP' lines have been deactivated, the 'SRP busy' line is no longer active. The 'block SRP end op trigger' may be on at this time, if the 'last card trigger' has turned it on. During any other operation than a last-card sequence (or a load operation), deactivating 'SRP busy' turns on the 'end operation' FF. The resulting level 4 response causes a level 4 interrupt request to the CPU.

After the 'XIO punch trigger' was turned off but before 'punch SRP' was deactivated, the 'card in punch station latch' was turned off. Therefore, another attempt to start punching, before the present card has been removed from the punch station, causes a feed cycle. The feed cycle can also be caused by a feed cycle instruction or a start read instruction.

Start Read (Models 6 and 7)

- Modifier bit 13 causes a start read operation.
- Start read operation cannot start unless the 1442 is ready, in which case there is a card in position to be read during the next feed cycle.
- Start read causes a feed cycle and sets the adapter so that read response interrupt requests occur for each column.
- Maintenance Diagrams XR511, XR711.

'Area 2 control' and 'U-register 15' allow a T4 pulse from the CPU to turn on both the 'XIO read trigger' and the 'XIO feed trigger.' If the motor is not running, it is necessary to start the motor and activate the 'SRP motor delay'line. Then 'SRP feed or program load' can turn on the 'feed clutch latch' and start a feed cycle.

Turning on the 'XIO read trigger' sets the adapter circuits to sense read emitter pulses. Reading and checking of a column of data starts. Then a read response activates a level 0 interrupt request. The operation for each column is completed by transferring the data to the CPU during execution of the interrupt servicing subroutine. This sequence is repeated for each column through column 80. Then a level 4 interrupt request occurs.

Reading and Checking a Column

- Read emitter pulse occurs while the read solar cells of the 1442 are sensing the holes punched in the column.
- Time 1 - time 2 sequence occurs twice for each column.
- The end of each time 2 causes a register complement sample pulse.
- The start of the second time 2 also causes a register complement sample pulse.
- The end of the second time 2 causes a read interrupt and error sample pulse.
- Then the final setting of the data register occurs.
- Maintenance Diagram XR511.

The active 'read emitter' and 'SRP read or program load' lines start the read check SS timing. The voltage shift when the SS starts turns on the 'time 1' FF and activates the SPD that causes a register reset sample pulse. The sample pulse resets (turns off) all of the data register flip-flops.

The 'register complement bit 0-9, 11, 12' lines corresponding to the holes in the column are active now. Turning 'time 1' off turns on the 'time 2' FF. Then, when 'time 2' turns off the first time for each column, the register complement sample pulses are activated. The sample pulse turns on each data register FF that is gated by an active register complement bit line.

The read check SS timing out starts the time 1-time 2 sequence again. This time the start of time 2 causes a register complement sample pulse. Only the data register FF's that were turned on by the first sample pulse should be affected. This is true because the same gating complement bit lines should be active. The effect should be that all data register FF's are off after the second sample pulse.

Turning off 'time 2' again activates a third register complement sample pulse. The readings from the solar cells again are set into the data register. However, at the same time as the register complement sample pulse, the end of time 2 also fires the SPD that activates the 'read interrupt and error SP'. Because of the requirement that the gate precede the set pulse, only a data register FF that was already on can cause the turn-on of the 'read error trigger'. Thus the data error check occurs before the final setting of the data register.

The 'read interrupt and error SP' also turns on the 'read response trigger', and the 'level 0 response' line causes an interrupt request in the CPU. The subroutine contains an instruction to transfer the data from the data register to CPU core storage. (See "Read.") The operation is repeated until after the 80th column has been read.

End Operation

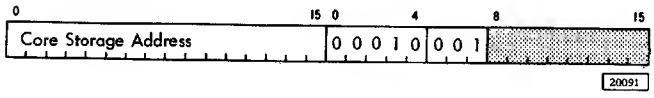
- The end of the busy condition turns on the 'end operation' FF.
- 'End operation response' sets a 1 in DSW position 4.
- 'Level 4 response' causes an interrupt request (level 4) in the CPU.

Turning off the 'feed CB 1-2' latch when feed CB 2 is activated turns off both the 'XIO read trigger' and the 'XIO feed trigger.' Turning off the latter FF deactivates the 'SRP busy' line. The resulting voltage shift turns on the 'end operation' FF, activating 'end operation response' and 'level 4 response.'

WRITE

- XIO instruction with a write function code in the IOCC loads the data register.
- The instruction must be given within approximately 300 microseconds of the punch response interrupt request.
- Maintenance Diagrams XR501, XR701.

The IOCC used with the XIO instruction to cause a write operation is:



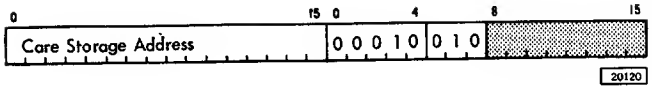
Activating the 'area 2' and 'XIO write' lines from the CPU can activate the 'load punch data' line at T4 of the E3 cycle. The operation can only occur, however, if the 1442 is ready and the 'punch gate SS' is timing. Activating 'load punch data' fires an SPD that activates 'load punch data SP'. The sample pulse turns on the data register FF's according to the CPU B-register FF's that are on.

The end of the T4 pulse that loaded the data register turns on the 'punch data trigger.' 'Punch data SRP' is activated and gates the data register outputs to control the punch magnets in the 1442. The gate ends when punch CB 2 turns off the 'punch CB 1-2' latch. Turning off this latch turns off the 'punch data trigger.'

READ

- XIO instruction with a read function code in the IOCC causes the transfer of data from the data register to the CPU.
- Instruction should be given within approximately 800 microseconds of the read response interrupt request for a model 6. The time is 700 microseconds for a model 7.
- Maintenance Diagrams XR511, XR711.

The IOCC used with the XIO instruction to cause a read operation is:



When the 'area 2' and 'XIO read' lines are activated by the CPU, two adapter lines are made active. The 'read area 2' line gates data register bits 3-9 inclusive, allowing them to activate the SRP data bit 5 through 11 lines, respectively. These bits are transferred in this manner in a read operation only (Figure 2-4).

The 'read A2 or program load' line is also activated and gates data register 12, 11, and 0-2 bits to activate the SRP data bit 0 through 4 lines. This transfer occurs for either a read operation or a program load operation.

CPU circuits control the setting of the B-register during the E3 cycle, and the consequent writing of core storage. The address word of the IOCC provides the address for storing the contents of the B-register. Updating of the address for each column must be performed by the program.

PROGRAM LOAD

- Pressing the CPU program load key starts the program load operation.
- Program load causes the feeding and reading of one card, reading all 80 columns.
- Read responses are prevented from causing interrupts in the CPU, but do cause a CPU cycle for each column.
- Card data is stored in locations /0000 through /004F of core storage.
- Each column is stored as a one-word instruction (Figure 2-6).
- No end operation interrupt request occurs. The CPU starts executing the instruction in location /0000.
- Maintenance Diagrams XR521, XR711.

The operation of the adapter during the program load operation is similar to a read operation. The major differences are in the effects on CPU operation resulting from using a 1442 for program loading.

Before starting a program load operation, the 1442 must have been made ready. Moreover, the CPU reset key must have been pressed, if the CPU clock (T6) has turned on the 'reset condition' FF. Although the name is misleading, the 'reset condition' FF must be off to allow turning on the 'program load' FF. With 'SRP ready' active, and the 'reset condition' FF off, pressing the program load key allows an oscillator A-pulse to turn on the 'program load' FF in the CPU.

Pressing the reset key also resets the instruction address register (IAR) to all 0's. IAR is used during the program load operation to address core storage. As each column's data is stored, IAR is incremented. Consequently, data from column 1 is stored at location /0000, from column 2 at location /0001, ..., from column 80 at /004F.

Turning on the 'program load' FF, through a jumper in the CPU, activates the 'program load to SRP' line. This line, in turn, activates lines in the adapter that accomplish the same functions as turning on the 'XIO read trigger' and the 'XIO feed trigger.' These functions are described in "Control" ("Start Read").

Reading and checking start as they do in a start read operation. Activating the 'level 0 response' (by turning on the 'read response trigger' in the adapter) activates the 'request interrupt level 0' line in the CPU. However, the 'gate interrupt' line cannot be activated during a program load operation. Therefore, the '(interrupt) level 0' FF is prevented from turning on.

At this time the data register contains data that has been read and checked. The CPU clock must be started so that the data can be stored in the location specified by IAR (Figure 2-9). Each phase B pulse, with the clock stopped at T7 during program load, activates the 'program load T7 phase B' line. This line is one means of activating the 'delay' line, which turns on the 'run' FF. However, the 'program load not SRP or PT response' line blocks the output of the 'run' FF so that no T-clock advance pulses can occur.

When 'level 0 response' deactivates the 'program load not SRP or PT response' line, the 'run' FF being on starts the T-clock. During the one clock cycle that occurs, the 'read response trigger' is turned off at T4. Therefore, the 'run' FF is prevented from causing another clock cycle until the next 'level 0 response.'

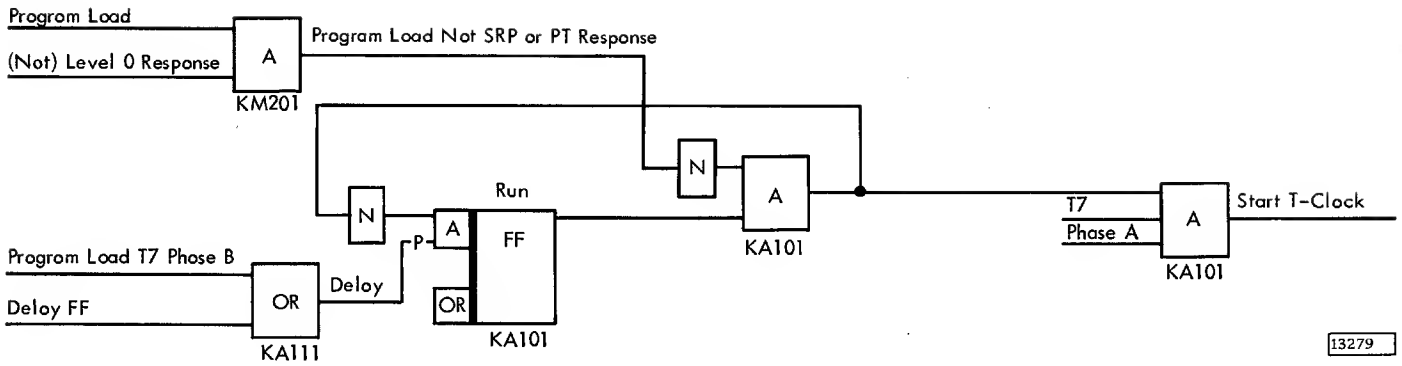


Figure 2-9. CPU T-Clock Control (1442 Program Load)

The CPU cycle timer has the 'I1' FF on, and does not advance during the data transfer cycles. The cycles taken are similar to I1 cycles, but certain of the normal functions are blocked. IAR addresses are transferred to the M-register to address core storage, and IAR is incremented +1, but transfers from the B-register to the operation register and D-register are blocked. 'Program load' activates 'entry gate' so that a T3 pulse can cause an 'I/O entry sample'. Data from the data register, in the adapter, then sets the CPU B-register. The write portion of the CPU cycle sets the data into the storage location addressed by the M-register.

The format in which the data is transferred for a program load operation is different from that for a programmed read operation. Figure 2-6 shows the significance of each punch row and the bit position of the core storage location that each row sets.

After all 80 columns have been read, checked, and transferred to core storage, the 1442 activates the 'feed CB-2' line to the adapter. The adapter transfers the signal to the CPU where it ANDs with 'program load' to activate the 'I/O reset IAR'. IAR is reset to address location /0000, and the 'DC reset IAR' line allows the end of the next oscillator A-pulse to turn off the 'program load' FF.

Turning off 'program load' allows the 'run' FF to start the CPU clock. Execution starts with the instruction read from column 1 and stored in location /0000.

Deactivating the 'SRP busy' line occurred before the CPU 'program load' FF was turned off. Therefore, the 'end operation' FF cannot turn on, and no level 4 (end operation) response occurs.

OPERATOR PANEL KEYS (1442)

- The operator panel is mounted on the 1442.
- Effect of the operator panel keys on the adapter circuits is described here.
- Description of operator panel lights is included in "Sense Device" ("Significance of DSW Bits," primarily "Error Check").

The start, stop, and nonprocess runout (NPRO) keys are mounted on the operator panel of the 1442.

Start

- Start key is pressed to turn on the 'start' latch in the adapter.
- 'Start' latch must be on to make the 1442 ready.
- Maintenance Diagram XR531, XR721.

Pressing the start key activates the 'start switch' line to the adapter if all these conditions are true.

1. Cover interlock in operating position.
2. Chip box in place and not full.
3. Stacker not full.
4. Stop key not being pressed.

If there is no 'SRP error' and there are cards in the hopper or a card in the read station, activating 'start switch' turns on the 'start' latch.

If 'SRP ready' and 'card in read station' are both inactive, the 'start' latch turns on the 'motor' latch. After approximately 850 ms, the 'feed clutch' latch can turn on, and a feed cycle results. The 'card in read station' latch is turned on by 'any lamp dark' during the time the 'feed interlock' latch is on. 'Start' latch on and 'card in read station' active turn on the 'ready' latch. The 'feed CB 3' line, when activated, turns off the 'start latch.

Stop

- Pressing the stop key removes the 1442 from the ready condition.
- Maintenance Diagram XR531.

Pressing the stop key activates the 'stop switch' line to the adapter, turning on the 'stop' latch. If the 1442 is busy, the 'stop latch is ineffective. However, at the end of the operation that is activating the 'SRP busy' line, the 'stop' latch turns off the 'ready' latch.

Nonprocess Runout

- Pressing the nonprocess runout key causes feed cycles without processing.
- All interrupts are blocked.
- Maintenance Diagram XR541.

Pressing the NPRO key turns on the 'NPRO latch' unless the 1442 is busy when the key is pressed. If the 1442 is busy, the key must be held until the present operation is completed and 'SRP busy' is deactivated. Then the 'NPRO' latch can turn on, activating both the 'NPRO' and the 'power reset or NPRO' lines.

The active 'NPRO' line turns on the 'motor' latch and the 'feed clutch' latch. The number of cycles that results depends on how long the NPRO key is pressed.

The 'power reset or NPRO' line turns off numerous controls throughout the adapter circuits. These are:

1. The 'ready' latch and 'start' latch. The 'start latch' is not likely to be on. Turning off the 'ready' latch prevents processing during the NPRO feed cycles.
2. The 'feed check' latches, 'misfeed' latch, and 'stacker jam' latch. All types of feed check errors are cleared.
3. The 'read error trigger' or 'punch error trigger.' All data check errors are cleared.
4. The 'process meter' latch. The 1442 process meter stops. The meter is restarted the next time the 1442 becomes busy.

FEATURES

There are no features available on the IBM 1442 Card Read Punch adapter.

POWER SUPPLIES AND CONTROL

Power for the IBM 1442 Card Read Punch adapter is provided and controlled by the CPU.

CONSOLE AND MAINTENANCE FEATURES

There are no console and maintenance features in the IBM 1442 Card Read Punch adapter. Operation of keys and lights of the 1442 operator panel is described in "Principles of Operation," Part 2 of this manual.

INTRODUCTION

FUNCTIONS OF THE IBM PAPER TAPE UNITS

- The IBM Paper Tape Reader and IBM 1055 Paper Tape Punch provide paper tape input and output, respectively, for the 1130 system.
- One of each can be connected to the system.
- The 1134 and 1055 operate under direct program control.
- The 1134 Paper Tape Reader reads 1-inch, eight-track paper tape at a maximum rate of 60 columns per second.
- When no card reader is included in the system, the 1134 provides a program load function.
- The 1055 Paper Tape Punch punches 1-inch, eight-track paper tape at a maximum punching rate of 14.8 columns per second.
- For additional 1055 information, see the IBM Field Engineering Manual of Instruction, 1054 Paper Tape Reader and 1055 Paper Tape Punch.
- For additional 1134 Paper Tape Reader information, see IBM Field Engineering Theory-Maintenance.

The 1134 Paper Tape Reader reads input data as an image of the holes in the tape. One paper tape character is read from each tape column. Any code translation must be made by programming, after the data is transferred to the CPU.

Figure 3-1 indicates which bits of the word correspond to the respective holes in the paper tape. In a program load operation only channels 1, 2, 3, and 4 are used, and four columns contain a complete instruction.

The 1055 Paper Tape Punch punches data as an image of the data contained in the core storage word on a character-to-character basis as shown in Figure 3-1.

Special data-character and control-character (feed code, etc.) coding and recognition must be handled by the stored program.

Although the adapter is described in this manual as a single adapter, an 1130 system can include either a paper tape reader or a paper tape punch without the other device.

ADAPTER CONTROLS

- Paper tape adapter is area code decimal 3 (00011).
- Decoding of the IOCC in the CPU selects the reader or punch device and defines the operation.
- Output data for the paper tape punch is provided to the adapter via the B-register.
- Adapter signals the selected device to start and control mechanical action.
- Reader and punch devices signal when they are ready.
- Adapter stores data from the reader for transfer to the CPU.
- Adapter provides responses (reader and punch) to the CPU.
- Adapter provides ILSW and DSW bits when sensed by CPU instructions.

Control signals from the CPU are recognized as applying to the paper tape adapter when the area code 3 is present in the IOCC. These signals define the operation to be performed by the adapter and device. Other lines from the CPU to the adapter supply timings and reset control as well as providing lines for the transfer of punch data.

Depending on the operation, the adapter then provides signals to the appropriate device -- reader or punch. These signals start mechanical action in the device. In a punch operation, the adapter punch buffer provides the data to be punched.

Lines from the devices to the adapter indicate when the device is ready. From the reader there are also lines used in setting the read buffer and/or the program load buffers.

Signal lines from the adapter to the CPU indicate a paper tape response and allow the sensing of other

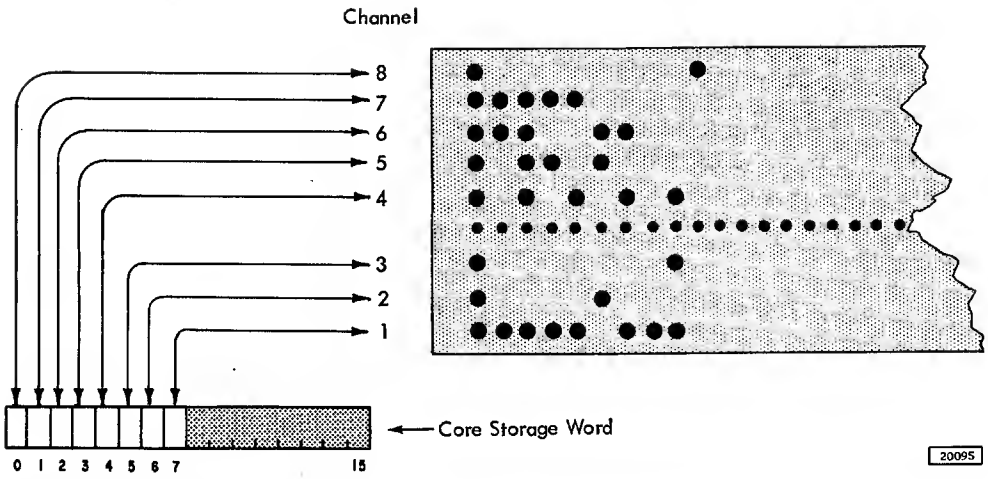


Figure 3-1. 1134/1055 Character Format

status conditions. These lines set 1's in the DSW or ILSW when the sense instruction is given. Other lines provide for the transfer of read or program load data.

FUNCTIONAL UNITS

TIMING CIRCUITS

- Oscillator (120 hertz) and its associated circuits provide timings for both the 1055 and the 1134.
- 'PT reader oscillator trigger' FF turns on and turns off once for each oscillation of the oscillator.

The paper tape adapter includes an oscillator with a frequency of 120 hertz. The oscillator controls timings for both the 1055 Paper Tape Punch and the 1134 Paper Tape Reader. The oscillator continually changes the state of the 'PT oscillator trigger' FF, turning it on and off for each oscillator cycle. The output of the FF is used in punch, read, and program load operations.

Punch Timing

- 'PT punch busy' FF is on.
- PT punch control timing ring runs.

When the 'PT punch busy' FF is on, the output gates the binary operation of the three paper tape control flip-flops. Each time the 'PT reader oscillator trigger' FF turns on, the state of 'PT punch control (A)' FF is changed. Turning off 'PT punch control (A)' FF changes the state of 'PT punch control (B) 'FF, and turning off 'PT punch control (B)' changes the state of 'PT punch control (C)' FF. Various outputs of the punch control flip-flops provide timings for paper tape punch operations.

Read Timing

- When gated, each cycle of the oscillator changes the state of the 'PT control trigger' FF.
- Turning on the 'PT control trigger' FF starts the PT reader SS timing.
- Outputs of the 'PT control trigger' control paper tape read timings.

The XIO control function instruction turns on the 'PT reader busy' FF and activates 'gate PT oscillator trigger.' With that line active, each oscillator cycle changes the state of the 'PT control trigger' FF. The voltage shift that occurs when that FF is turned on starts the timing of the 500 microsecond singleshot. The SS assists in timing read operations.

Another output turns off the 'inhibit PT response' FF, after the FF has blocked the first response of the PT reader operation. Still other outputs AND with 'PT reader oscillator trigger' outputs to gate the reader clutch and sensing contacts.

Program Load Timing

- 'PT control trigger' and PT reader SS functions are like those during PT reader operations.

- Additionally, the 'PT program load 1' and 'PT program load 2' flip-flops time the loading of the program load and read buffers.

In a program load operation, the 'PT program load 1' FF can be turned on if both these conditions are true:

1. No punch in channel 6 or 7 is sensed.
2. 'PT program load 2' FF is also off.

Under these conditions, the 'set PT read buffer' pulse turns on 'PT program load 1' and sets the program load 1 buffer with the data being sensed.

The next 'set PT read buffer' pulse turns on the 'PT program load 2' FF. However, the FF is not on in time to cause loading of program load 2 buffer. The data being sensed is set into the read buffer. 'PT program load 2' blocks the subsequent 'set PT read buffer' pulses, until the flip-flop is turned off.

Timing out of the PT reader SS, with both 'PT program load 1' and 'PT program load 2' on, activates the 'set program load buffer' pulse. This pulse sets program load 2 buffer with the data being sensed, then turns off the 'PT program load 1' FF. The 'PT program load 2' FF remains on until T6 of the CPU cycle that transfers the complete instruction to core storage.

PUNCH BUFFER

- Eight-position punch buffer is set from the CPU B-register with data to be punched.

The eight flip-flops of the punch buffer are initially reset (turned off) by a 'DC reset 3' line from the CPU. When the instruction to punch is given, the 'PT punch busy' FF turns on. Turning the FF on activates the 'set PT punch buffer' pulse. Punch buffer flip-flops turn on according to the contents of the CPU B-register at that time.

After controlling energization of the paper tape punch magnets, all flip-flops of the punch buffer are turned off. This is done by the 'reset PT punch buffer' line, activated when both 'PT punch control (B)' and 'PT punch control (C)' are on.

READ BUFFER

- All flip-flops are reset to the on state.

- Read buffer is reset when the PT reader SS starts timing.

- When the singleshot times out, each flip-flop is turned off if there is no corresponding hole in the tape.

- In a read operation, data from channel 1 through 8 is gated from the read buffer to B-register 7 through 0 positions, respectively, during data transfer.

- In a program load operation, the read buffer positions with data from channels 1 through 4, only are transferred.

In a read operation, each time the PT reader SS starts timing, 'reset PT read buffer's is activated. This line turns on all eight flip-flops in the read buffer. When the singleshot times out, 'set PT read buffer' is activated. Any reader contact that is not sensing a hole in the tape is gating the turn-off of a flip-flop. The result is that, after the set pulse, the read buffer has its FF's left on to correspond with the data sensed.

The operation of the read buffer during program load differs in that the 'PT program load 2' line blocks both the reset and set. The read buffer retains the data that becomes bit positions 4 through 7 of the instruction transferred to the CPU.

PROGRAM LOAD BUFFERS

- Program load buffer 1 and program load buffer 2 each have four positions.

- Program load buffer 1 stores data from the first of four columns that contain an instruction.

- Program load buffer 2 stores data from the third of four columns that contain an instruction.

- All positions of both buffers are turned off (reset) once for each instruction in the program tape.

- All positions of both buffers are turned off (reset) when IAR in the CPU is reset at the end of a program load operation.

Before the 'PT program load 1' FF is turned on, if there is no punch in channel 6 or 7, 'reset PT read buffer'causes a 'binary reset program load buffers' pulse. This pulse turns off all the flip-flops in both program load buffers. Then activating 'PT program load 1' turns on the program load buffer 1 flip-flops that are gated by sensing holes in the tape.

Later, activating 'set program load buffer' turns on the program load buffer 2 flip-flops that are gated by holes inthe tape. The 'set program load buffer' pulse is the same pulse that turns off the 'PT program load 1' FF.

Thus, at the time of transfer to the CPU, the program load buffers contain eight bits of the instruction to be transferred. These bits are stored in positions 0-3 and 8-11 of the addressed core storage position.

The program load buffers are both reset again by the 'dc reset IAR' pulse. This pulse occurs at the end of the program load operation, when execution of the program just loaded is to start.

PRINCIPLES OF OPERATION

- The paper tape adapter initiates action by the 1055 or the 1134 as the result of an XIO instruction in the CPU program.
- The area code for the paper tape units is decimal 3 (00011).
- Function codes that are applicable are:

  'Sense interrupt'
  'Sense device'
  'Write' (1055 Paper Tape Punch)
  'Control' (1134 Paper Tape Reader)
  'Read' (1134 Paper Tape Reader)

- If the system includes no card reader, the paper tape adapter controls a program load operation that results from pressing the CPU program load key.

SENSE INTERRUPT (011)

- Sense Interrupt sets an interrupt level status word (ILSW) in the accumulator of the CPU.
- No area code is required in the IOCC.
- ILSW is set for the highest level of interrupt active when the instruction is given.
- Paper tape devices interrupt on level 4.

An XIO instruction with a function code of sense interrupt activates the 'XIO sense ILSW' line from the CPU. If 'interrupt level 4' is active when the instruction is given, 'paper tape response' can activate the 'paper tape ILSW bit 0 ' line. Bit 0 in the ILSW indicates that one of the paper tape devices has requested an interrupt.

SENSE DEVICE (111)

- Sense device sets the device status word (DSW) in the accumulator of the CPU.
- Status conditions of the paper tape devices or the adapter result in 1's in the DSW during the CPU E2 cycle.
- Bit 15 in the IOCC turns off the paper tape reader response.

An XIO instruction with a sense device function code in the IOCC activates the 'XIO sense device' line from the CPU. The line is activated and gates the DSW bits during the E2 cycle in the CPU. The IOCC for the sense device operation (paper tape devices) is:

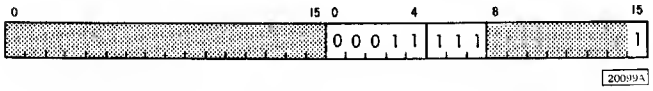


Figure 3-2 shows the DSW that is set in the accumulator for the paper tape (PT) devices. Either the punch response or the reader response shown causes an interrupt request to the CPU.

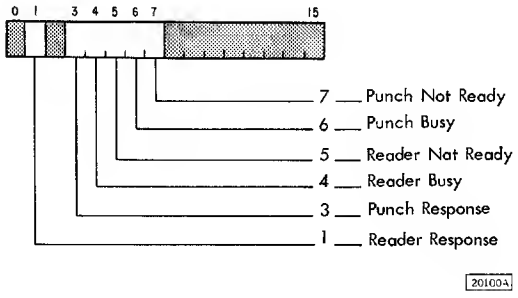


Figure 3-2. Device Status Word (1134/1055)

Significance of DSW Bits

Reader Response (Bit 1): A 1 in this position indicates the 'PT reader response' FF is on and data is ready for transfer to the CPU. The 'PT reader response' FF is turned on at the same time the read buffer is set with the data from a tape column. This FF being on is one way of activating 'PT response', causing an interrupt request to the CPU.

Punch Response (Bit 3): A 1 in this position indicates the 'PT punch response' FF is on. The FF is turned on when the PT punch is no longer busy after punching a tape column. The contents of the punch buffer have been cleared (reset), and the instruction to punch another column can be given. 'PT response' causes an interrupt request to the CPU.

Reader Busy (Bit 4): A 1 in this position indicates the 'PT reader busy' FF is on or the 'gate response PT reader' line is active. The FF is turned on when reading of a column is started by an 'XIO control' function. Turning on 'PT reader busy' activates the 'gate response PT reader' line, which turns on a second FF (PT status busy). Both flip-flops remain on until the 500 microsecond PT reader SS times out.

'Reader busy' also sets a 1 in position 5 of the DSW.

Reader Not Ready (Bit 5): A 1 in this position indicates that the 'PT reader ready' line from the 1134 is not active or the reader is busy. The 'PT reader ready' line is deactivated when the tape tension switch in the device is open. Manual intervention by the operator is required, because the tape is broken or not feeding freely.

This condition should be tested by the program before a read command is given. If a 'read' command is given while this condition exists, erroneous data can be transferred to the CPU. No valid indication is given as to whether the data read is correct or incorrect.

Punch Busy (Bit 6): A 1 in this position indicates that the 'PT punch busy' FF is on. The FF is turned on at the start of a punch operation (at T6, when 'XIO write' and 'area 3' are active). The 'PT punch busy' FF remains on until the 'PT punch control C' FF is turned off.

'Punch busy' also sets a 1 in position 7 of the DSW.

Punch Not Ready (Bit 7): A 1 in this position indicates that the 'PT punch ready' line from the device is not active or that the punch is busy. The 'PT punch ready' line is deactivated when any one of these conditions exists:

1. Tape is not feeding freely from the tape spool.
2. Tape pressure roll holder is not down and holding the tape against the feed wheel.
3. There is no tape in the PT punch device.

Manual intervention is required to clear these conditions.

This status should always be tested by the program before a write command is given. If the write command is given while this indicator is on, loss of information occurs. No indication is given of this loss.

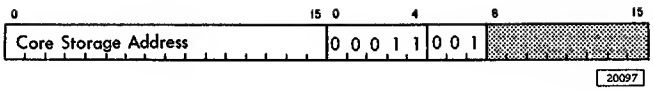
Sense Reset

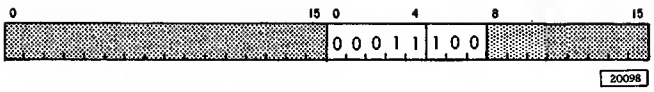
Modifier bit 15 = 1 in the IOCC turns off the PT response that is activating a level 4 interrupt request. In the CPU, modifier bit 15 activates the 'XIO sense reset 15' line. When 'area 3' is also active, a T6 pulse blocks the dot AND that activates the 'PT response' line. The resulting voltage shift turns off 'PT punch response' if the 'B bit 3' line is active. If 'B bit 1 or program load' is active, the voltage shift turns off the 'PT reader response' FF.

WRITE (001)

- An XIO instruction with a write function code in the IOCC causes punching in one column of the tape and advancement of the tape.
- A punch response causes a PT response interrupt request to signal that the next punch operation can be started.
- Maintenance Diagrams XT511, XT711.

During the E3 cycle in the CPU, the character to be punched is read from core storage and set into the B-register. The address word of the IOCC selects the core storage position that is read. When multiple columns are to be punched, the program must update the address for each character. The IOCC for a write function is:





At T6 of the CPU cycle, activation of 'XIO write' and 'area 3' turns on the 'PT punch busy' FF. This flip-flop gates the operation of the PT punch control timing ring and activates 'set PT punch buffer.' The character from B-register positions 0-7 is set into the punch buffer. Punch buffer outputs then control energization of the punch magnets.

Turning on 'PT punch control A' FF turns on the 'clutch drive' FF. If the PT punch is ready, the clutch magnet can now be energized to start mechanical operation of the punch drive. The 'clutch drive' FF stays on until turned off by turning off 'PT punch control B' FF for the first time.

While 'PT punch control B' is on the second time and 'PT punch control C' is also on, 'reset PT punch buffer' is active. This line clears the character from the punch buffer.

Turning off 'PT punch control C' FF results in turning off the 'PT punch busy' FF. Deactivating the 'PT punch busy' line turns on the 'PT punch response' FF. Punch response is one of the ways to cause a PT response interrupt request (level 4) to the CPU.

CONTROL (100)

- XIO instruction with a 'control' function code in the IOCC precedes the paper tape read operation for each column.
- Read buffer is reset and loaded with the tape image.
- Read response causes a level 4 PT response interrupt request.
- Tape is moved to the next character position.
- First control command after the PT reader is made ready only moves the tape. The read buffer is not loaded and no reader response occurs.
- Maintenance Diagrams XT501, XT701.

The IOCC for the control function that must precede the read operation for each column is:

A T6 pulse turns on the 'PT reader busy' FF, when the reader is ready and 'XIO control' and 'area 3' lines are active. The 'PT reader busy' FF being on activates both the 'PT reader busy' line and the 'gate PT oscillator trigger' line. The latter line allows the oscillator to turn on the 'PT control trigger' FF. The oscillator then turns the 'PT control trigger' off after one oscillator cycle (approximately 8.5 ms).

The 'PT control trigger' being on allows the on condition of the 'oscillator trigger' to activate 'gate PT contacts common', 'PT reader clutch drive A', and 'PT reader clutch drive B.' 'Gate PT contacts common' must be active to allow loading the read buffer. Actual tape motion cannot start immediately so the contacts can continue to sense the holes in the tape.

Turning on the 'PT control trigger' starts the 500-microsecond PT reader SS. The start of its output activates the 'reset PT read buffer' line. The PT reader SS timing out activates the 'set PT read buffer' line, loading the read buffer with the tape image. The singleshot timing out also turns on the 'PT reader response' FF and turns off the 'PT reader busy' FF.

The timing chart (XT701) shows the effect of giving a second 'XIO control' instruction before tape motion has been completed. The 'PT reader busy' FF was turned off when the PT reader SS timed out, but the second instruction turns 'PT reader busy' back on. However, the SS cannot be restarted, because to do so requires the turning on of the 'PT control trigger.' The 'PT control trigger' must be turned off and back on to start the PT reader SS timing again. 'PT reader busy' stays on until the second character can be set into the read buffer.

Inhibit PT Response

The first control function after the PT reader is made ready does not cause loading of the read buffer. Neither does a PT reader response occur. Activating the 'PT reader ready' line turns on the 'inhibit PT response' FF. The output of this FF blocks the output of the PT reader SS from being completely effective. Only 'reset PT read buffer' is activated, and only paper tape motion results from the first control function. Turning off the 'PT control trigger

turns off 'inhibit PT response', and it is not turned on again.

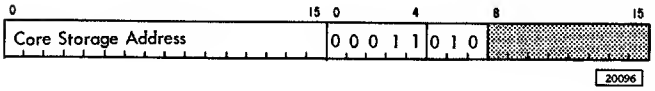
Block Channel 5

In a program load operation, a punch in channel 5 terminates the program load operation. However, in a read operation, channel 5 must be handled as any other channel. The 'gate channel 5' line must be held inactive by turning on the FF, which could be called the block channel 5 FF. Activating 'gate PT oscillator trigger' turns on the block channel 5 FF, and it remains on throughout a read operation.

READ (010)

- XIO instruction with a 'read' function code in the IOCC is given in the interrupt servicing subroutine.
- Read buffer data is transferred to core storage via the CPU B-register.
- Maintenance Diagrams XT501, XT701.

During the E3 cycle in the CPU, the 'XIO read' and 'area 3' lines to the adapter become active. The IOCC is:



As a result, 'gate PT entry' is activated and the outputs of the read buffer can set the CPU B-register. At write time of the E3 cycle, the contents of the B-register enter core storage.

PROGRAM LOAD

- Paper tape reader can load a program when no card reader is included in the system.
- Pressing the CPU program load key starts the program load operation.
- Delete code leader feeds without reading.
- Each instruction is made up of data from four tape columns. Channels 1-4 only are used.
- Four positions of each instruction are set into the read buffer, and eight positions are set into the program load buffer.
- After each group of four columns have been read, a reader response causes a CPU cycle, but no interrupt request.
- CPU cycle transfers the contents of both buffers to core storage via the B-register.
- Instructions are stored in /0000 and progressively higher address locations. IAR provides the addresses.
- Reading stops when a channel 5 punch is sensed.
- IAR is reset to /0000, and execution of the instruction at that address starts.
- Maintenance Diagrams XT501, XT721.

Pressing the program load key on the CPU keyboard activates the 'program load to PT' line, if the jumpers are installed to provide paper tape program loading. As a result, 'program load' lines in the adapter are activated to start and control the operation.

If 'PT reader ready' is active, 'program load drive' becomes active and, in turn, activates 'gate PT oscillator trigger.' Then, every other oscillation turns on the 'PT control trigger,' gating the reader contacts and energization of the reader drive clutch. The 'PT control trigger' turning on starts the PT reader SS. Activating 'gate PT oscillator trigger' turns on the 'block channel 5' FF so that sensing a channel 5 punch cannot end the program load operation.

Sensing delete codes (all punches) in the leader causes tape feeding without loading the program load buffer. Sensing a punch in channel 6 or channel 7 blocks the 'gate program load 1' line. 'Program load 1' FF cannot be turned on to allow loading the program load buffer. Neither can 'block channel 5' be turned off. Only a paper tape advance occurs for each column.

When the first column that has no channel 6 or 7 punch is read, 'gate program load 1' becomes active. The PT reader SS starting resets both read

and program load buffers. Timing out of the single-shot activates 'set PT read buffer,' which turns on the 'PT program load 1' FF. Turning on the 'PT program load 1' FF sets the data into program load buffer 1.

Timing out of the PT reader SS, with 'gate program load 1' active, also turns off the 'block channel 5' FF, so that sensing a channel 5 punch later can end the program load operation.

After setting the program load buffer 1 from the first column of the group of four columns that contain an instruction, the paper tape advances. When the PT reader SS times out for the second column, the 'set PT read buffer' line sets the data being sensed into the read buffer. The same line turns on the 'program load 2' FF. Another tape advance allows sensing the third column.

Timing out of the reader SS for the third column causes setting of the data into program load buffer 2. 'Program load 1' FF is turned off, and the tape advances to the position for sensing the fourth column of the group of four. Turning off 'program load 1' with 'program load 2' on then activates the 'gate response PT reader' line.

When the reader SS times out for the fourth column, 'program load 2' is turned off and the 'PT reader response' FF is turned on. At this time data from the first column (of the group of four columns forming an instruction) remains in the program load buffer 1. Data from the second column remains in the read buffer. Data from the third column remains in program load buffer 2. Data from the fourth column is present on the I/O bus, available for setting B-register position 12-15 (Figure 3-3).

The CPU clock must be started so that the data can be stored in the location specified by IAR (Figure 3-4). Each phase B pulse, with the clock stopped at T7 during program load, activates the 'program load T7 phase B' line. This line is one means of activating the 'delay' line, which turns on the 'run' FF. However, the 'program load not SRP or PT response' line blocks the output of the 'run' FF so that no T-clock advance pulses can occur.

When 'PT response' deactivates the 'program load not SRP or PT response' line, the 'run' FF being on starts the T-clock. During the one clock cycle that occurs, the 'PT reader response' FF is turned off at T6. Therefore, the 'run' FF is prevented from causing another clock cycle until the next 'PT response'.

The CPU cycle timer has the 'I1' FF on, and does not advance during the data transfer cycles. The cycles taken are similar to I1 cycles, but certain of the normal functions are blocked. IAR addresses are transferred to the M-register to

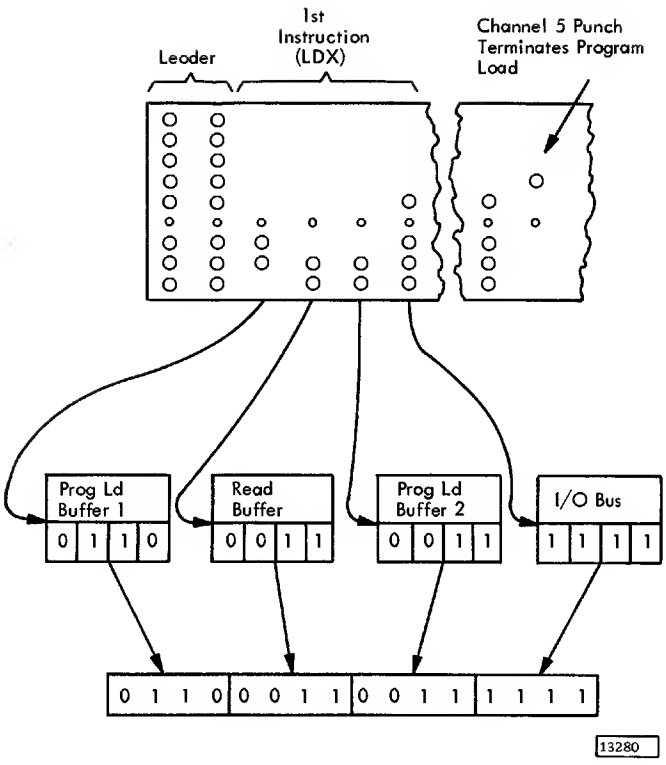


Figure 3-3. Program Load Data Flow

address core storage and IAR is incremented +1, but transfers from the B-register to the operation register and D-register are blocked. 'Program load' activates 'entry gate' so that a T3 pulse can cause an 'I/O entry sample'. Data from the adapter then sets the CPU B-register. The write portion of the CPU cycle sets the data into the storage location addressed by the M-register.

The format in which the data is transferred for a program load operation is different from that for a programmed read operation. Figure 3-3 shows the significance of each channel and column of the tape and the position of the core storage location that each punch sets.

The sequence of reading four tape columns and transferring the data to CPU core storage is repeated until a column that contains a channel 5 punch is sensed. (A delete character after setting the program load buffer 1 the first time can end the program load operation. The 'block channel 5' FF was turned off at that time.)

'Gate channel 5' and adapter 'PT channel 5' activate the 'PT channel 5' line to the CPU. There, this line ANDs with 'program load' to activate the I/O reset IAR'. IAR is reset to address location /0000, and the 'DC reset IAR' line allows the end of the next oscillator A-pulse to turn off the program load' FF.

Turning off 'program load' allows the 'run' FF to start the CPU clock (Figure 3-4). Execution starts with the instruction read from column 1 and stored in location /0000. No PT response interrupt request occurs.

FEATURES

There are no features available for either the IBM 1055 Paper Tape Punch or the IBM 1134 Paper Tape Reader.

POWER SUPPLIES AND CONTROL

Power for the IBM Paper Tape adapter is provided and controlled by the CPU.

CONSOLE AND MAINTENANCE FEATURES

There are no console and maintenance features in the IBM Paper Tape Adapter.

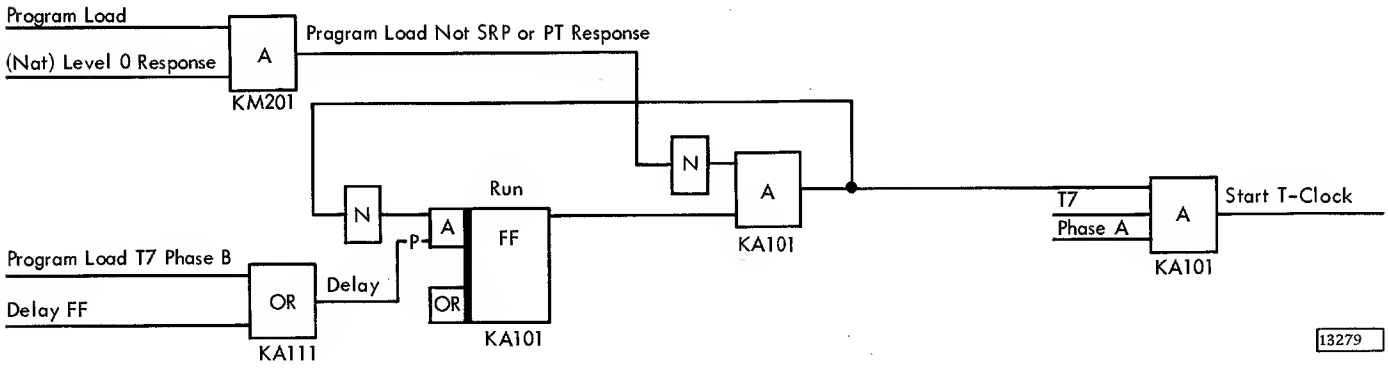


Figure 3-4. CPU T-Clock Control (PT Program Load)

INTRODUCTION

FUNCTIONS OF THE IBM 1627 PLOTTER

- The IBM 1627 Plotter provides graphic output of system data.
- One 1627 can be attached to a system.
- The 1627 operates under direct program control.
- For information on the plotter see the IBM Field Engineering Instruction-Maintenance Manual, 1627 Plotter. (See Bibliography.)

The IBM 1627 Plotter provides an exceptionally versatile, reliable, and easy-to-operate plotting system for the IBM 1130 Computing System. The plotter converts information from core storage via the adapter into graphic form. Bar charts, flow charts, organization charts, engineering drawings, and maps are among the many graphic forms of data which can be plotted on the 1627 Plotter.

Two models of the 1627 are available and the major characteristics are:

Model 1 -- Plotting area: 11 inches by 120 feet, 1/100-inch incremental-step size, 18,000 steps/minute.
Model 2 -- Plotting area: 29-1/2 inches by 120 feet, 1/100-inch incremental-size. 12,000 steps/minute.

More information on both models is given in Figure 4-1.

Speed	X, Y Increments Pen Status Change	Model 1 18,000 Steps/Min 600 Operations/Min	Model 2 12,000 Steps/Min 600 Operations/Min
Increment Size		1/100 Inch	1/100 Inch
Chart Paper	Width Plotting Width Length Sprocket Hole Dimensions	12 Inches 11 Inches 120 Feet .130 Inch Dia on 3/8 Inch Centers	31 Inches 29 1/2 Inches 120 Feet .188 Inch Dia on 1 Inch Centers

15667

Figure 4-1. Operating Characteristics (1627)

Under direct program control, data from core storage is transferred serially through the adapter. There it is translated into 1627 actuating signals. These signals control drawing movements by the 1627 Plotter.

The actual recording is produced by incremental movements of the pen on the paper surface (y-axis) and/or the paper under the pen (x-axis). The pen is mounted in a carriage that travels horizontally across the paper as viewed from the front of the plotter. The vertical plotting motion is achieved by rotation of the pin feed drum. The drum also acts as a platen (Figure 4-2).

Motion of the drum and the pen carriage is bi-directional; that is, the paper can move up or down, and the pen can move right or left. Control is also provided to raise or lower the pen from or to the paper surface. The pen remains in the raised or lowered position until directed to change to the opposite status.

ADAPTER CONNECTIONS

- The plotter adapter is selected by area code decimal 5 (00101).
- Function code lines from the CPU are 'XIO sense device' and 'XIO write.'

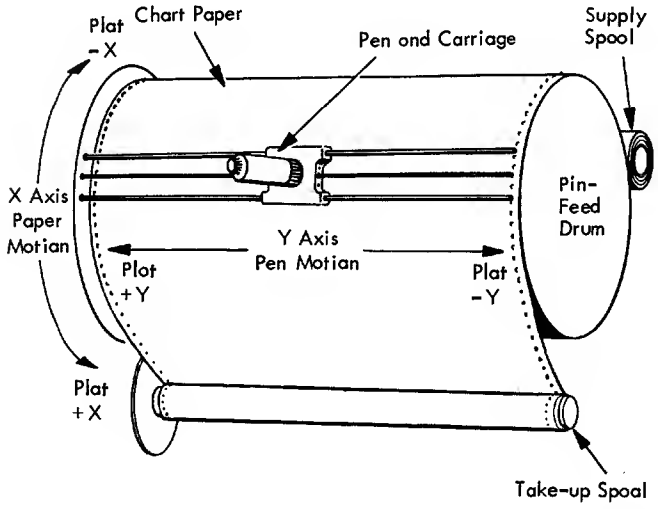


Figure 4-2. Drum and Pen Motions

- Certain B-register outputs gate the setting of the operation buffer in the adapter.
- Drive lines from the adapter to the 1627 control pen, carriage, and drum motion.
- Signal lines from the adapter to the CPU indicate the plotter response and other DSW bits, not ready or busy.

PLOTTING OPERATION

- Plotting operation results from executing a series of XIO instructions.
- IOCC for each instruction contains a write function code.
- Word transferred for each instruction defines the motion that is to take place.

Each XIO write instruction transfers six bit positions (0-5) of the addressed word to the operation buffer in the adapter. These bits are decoded, in the adapter, into a directional signal which causes a 1/100 inch incremental movement of the pen carriage (Figure 4-3) and/or drum, or a raise-pen or a lower-pen movement. The motion or action resulting from each code in the output record is shown in Figure 4-4.

The time required for execution of raise-pen and lower-pen commands is 100 ms. The time for each incremental-step for a model 1 is approximately 3.3 milliseconds. For a model 2, the time is approximately 5 ms.

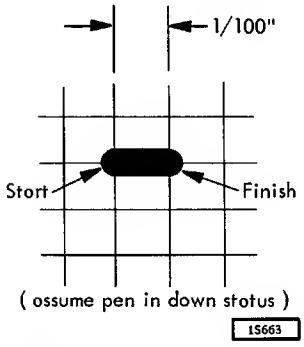


Figure 4-3. Result of One Horizontal (Y-Axis) Movement

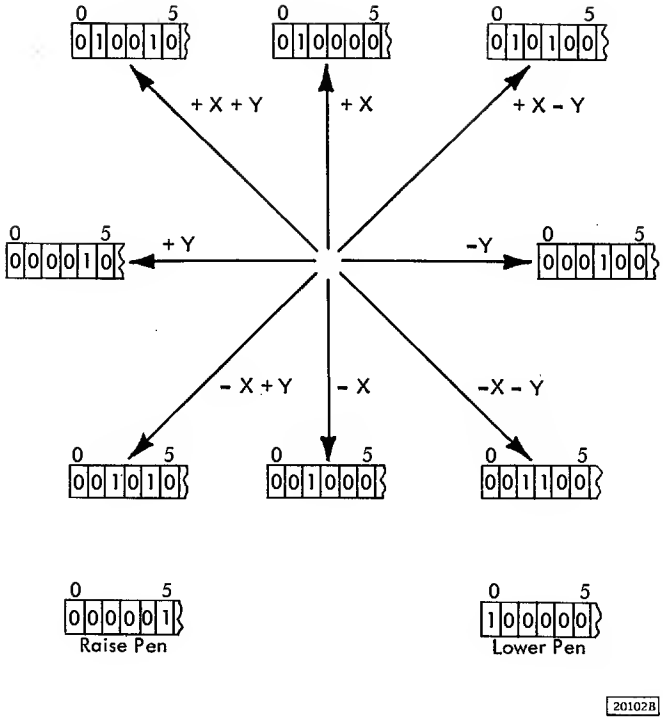


Figure 4-4. Output Record Control

FUNCTIONAL UNIT

OPERATION BUFFER

- Operation buffer contains six flip-flops, one for each function of the plotter.
- Flip-flops are reset off, and they can be turned on during a CPU E3 cycle.
- Buffer outputs activate control lines to the 1627 device.

The turn-on of each flip-flop is gated by a line from the CPU B-register. If the 'B bit' line is active, T6 of the CPU cycle in which 'area 5' and 'XIO write' are also active turns on the corresponding flip flop.

The output of each FF activates a line to the 1627, starting some motion of the pen, carriage, or drum. Then the FF is turned off by the timing out of a singleshot.

PRINCIPLES OF OPERATION

- The plotter adapter initiates action by the 1627 as the result of an XIO instruction in the CPU program.
- The area code for the 1627 is decimal 5 (00101).
- Sense interrupt function is applicable only when SAC II or customer devices in the system interrupt on level 3.
- Other function codes that are applicable are:

  'Sense device'
  'Write'

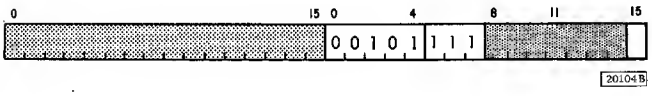
SENSE INTERRUPT (011)

- Sensing of the ILSW is required only if one or more other devices in the system cause level 3 interrupt requests.
- Area code is not required in the IOCC.
- If sense interrupt is required, the 1627 adapter provides a 1 in ILSW bit position 0.

SENSE DEVICE (111)

- Sense device function code in the IOCC of an XIO instruction causes setting of the DSW in the accumulator.
- DSW is set during a CPU E2 cycle.

The IOCC that is used is:



The DSW that is set in the accumulator during the E2 cycle in the CPU is shown in Figure 4-5.

Significance of DSW Bits

Plotter Response (Bit 0): A 1 in this position indicates that the 'response' FF in the plotter adapter is on. This condition activates the 'level 3 interrupt request' line in the CPU.

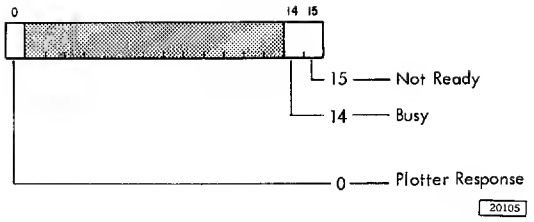


Figure 4-5. Device Status Word (1627)

Busy (Bit 14): A 1 in this position indicates that one of the four singleshots is timing. Any one of the singleshots that are started when a plotter operation starts can indicate busy.

Not Ready (Bit 15): A 1 in this position indicates that the 1627 is not activating the '-24V ready' line.

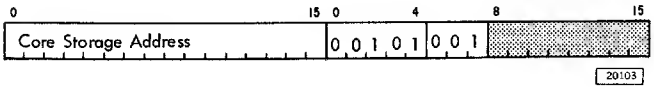
Sense Reset

Modifier bit 15 = 1 in the IOCC of a sense device command activates the 'XIO sense reset 15' line from the CPU. This line active, along with 'XIO sense device' and 'area 5' active, causes a reset pulse for the 'response' FF in the adapter. At the same time, 'I/O bit 0' must gate the turnoff. 'I/O bit 0' is active when the 'plotter DSW bit 0' is active.

WRITE (001)

- XIO instruction with a write function code in the IOCC causes the high-order six positions of the addressed word to set the operation buffer in the adapter.
- Each active buffer output line starts a function of the plotter.
- Singleshots later turn off the buffer flip-flops and, still later, turn on the 'response' FF, causing a level 3 interrupt request.
- Maintenance Diagrams XG501, XG701.

The IOCC for the write function is:



During the E3 cycle of the CPU, 'XIO write' and 'area 3' are activated. T6 turns on the operation buffer flip-flops that are gated by active B bit lines. The flip-flops are:

'Pen up' and 'pen down'.
'Drum up' and 'drum down'.
'Carriage right' and 'carriage left'.

Turning on the flip-flop activates the drive line to start motion described by the name of the flip-flop.

Turning on any flip-flop also starts the timing of the first of two singleshots in series. (When the first SS times out, the second SS starts timing.) The starting of the second SS turns off the flip-flop that started the timing sequence.

Drum and carriage control flip-flops use the busy singleshots 1 and 2. Their pulse duration for a model 1 is approximately 1.9 ms, and for a model 2 is approximately 2.9 ms. 'Pen up' and 'pen down' FF's start the timing of singleshots 3 and 4, each of which has a duration of approximately 50 ms.

When the second SS (2 or 4) times out, the voltage shift turns on the 'response' FF, activating 'plotter response'. This line to the CPU causes a level 3 interrupt request.

After the first 'write' command the program should wait for succeeding plotter interrupts to issue 'write' commands. If a 'write' command is given while busy is on, loss of information will probably occur. No indication of this loss is given.

FEATURES

There are no features available for the IBM 1627 Plotter adapter.

POWER SUPPLIES AND CONTROL

Power for the IBM 1627 Plotter adapter is provided and controlled by the CPU

CONSOLE AND MAINTENANCE FEATURES

There are no console and maintenance features in the IBM 1627 Plotter adapter.

INTRODUCTION

FUNCTIONS OF THE STORAGE ACCESS CHANNEL

- Storage access channel (SAC) provides the data, control, and timing lines required for attaching additional equipment to the 1130 system.
- An IBM 1133 Multiplexer Control Enclosure or an IBM 2250 Display Unit Model 4 uses the SAC (Figure 5-1).
- User-supplied equipment also uses the SAC for connection to the system.

The storage access channel functions as an extension or expansion of the CPU, allowing the connection of additional I/O devices. The SAC consists of lines that provide timings and control of the devices so that data can be transferred between the device and the CPU. Data transfer can be in either of the usual modes.

1. Cycle Steal Mode. An XIO instruction, with an initiate read or initiate write function, gives control of the data transfers to the SAC. When the SAC transfers words to or from core storage, CPU T-clock cycles are stopped and cycle steal cycles are taken. The CPU program has no control of or awareness of the cycle steal cycles.
2. Interrupt Mode. The external device can cause an interrupt of the CPU program by activating an interrupt request on level 2, 3, 4, or 5. The interrupt request must be serviced by the program, the same as an interrupt request by a basic device, for which the adapter is in the CPU.

Each device that uses the SAC must be assigned an area code, which must be different from that of any other device in the same system. Moreover, each device must be assigned to an interrupt level (2-5), and have a bit position reserved in the ILSW for that level. The ILSW bit position must not be the same as that for another device on that level.

In the execution of an XIO instruction by a device using the SAC, the control word of the IOCC is decoded in the device circuits. This difference in the handling of the IOCC is the major difference between devices using the SAC and the basic I/O devices. The SAC and the SAC adapter provide the necessary lines of communication between the CPU and the I/O devices.

ADAPTER CONNECTIONS

- Distinction between CPU and SAC adapter circuits cannot be made.
- Storage access channel and adapter data flow is shown in Figure 5-2.

Many of the lines which make up the storage access channel cable pass through the adapter with no change (Figure 5-2). The connections are those needed to allow the exchange of data between the CPU and the external device connected to the SAC. Besides timing pulses from the CPU, control lines are required in both directions. Depending on the device, data lines may be required from the CPU, to the CPU, or in both directions.

FUNCTIONAL UNITS

There are no functional units, as such, included in the SAC adapter. The logic involved gates the exchange of data and control between the CPU and the device.

The SAC consists of communication lines between the CPU and the devices using the SAC. Descriptions of these lines follow.

CPU TO DEVICE LINES

CPU Clock Times: The even-numbered clock times (T-clock) and phase A pulses are supplied to the devices via the SAC to allow the devices to synchronize with the CPU (in cycle steal operations).

Cycle Steal Clock Times: The even-numbered cycle steal clock times (X-clock) and phase A pulses are

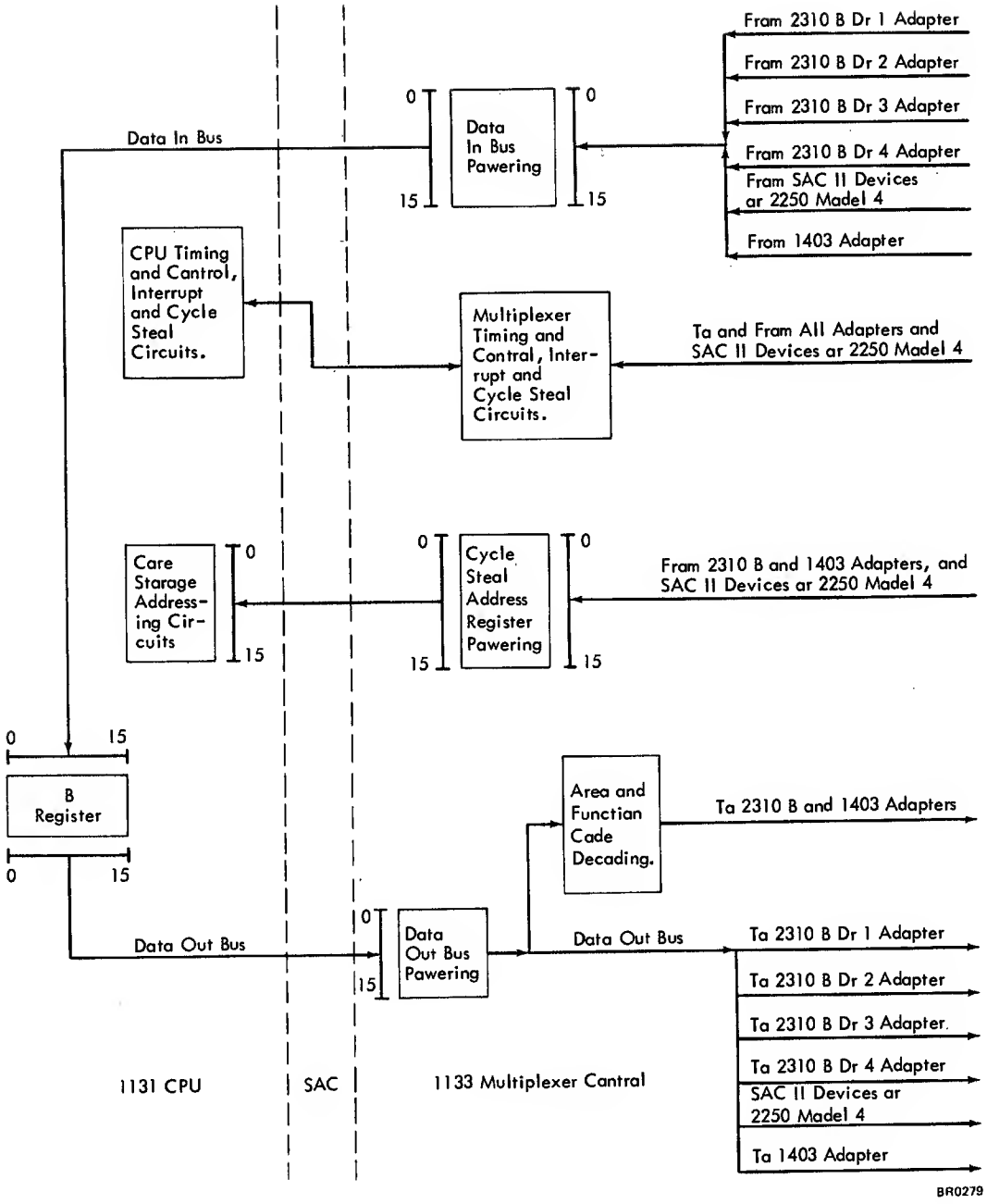


Figure 5-1. Miltiplexer Data Flaw Through the SAC

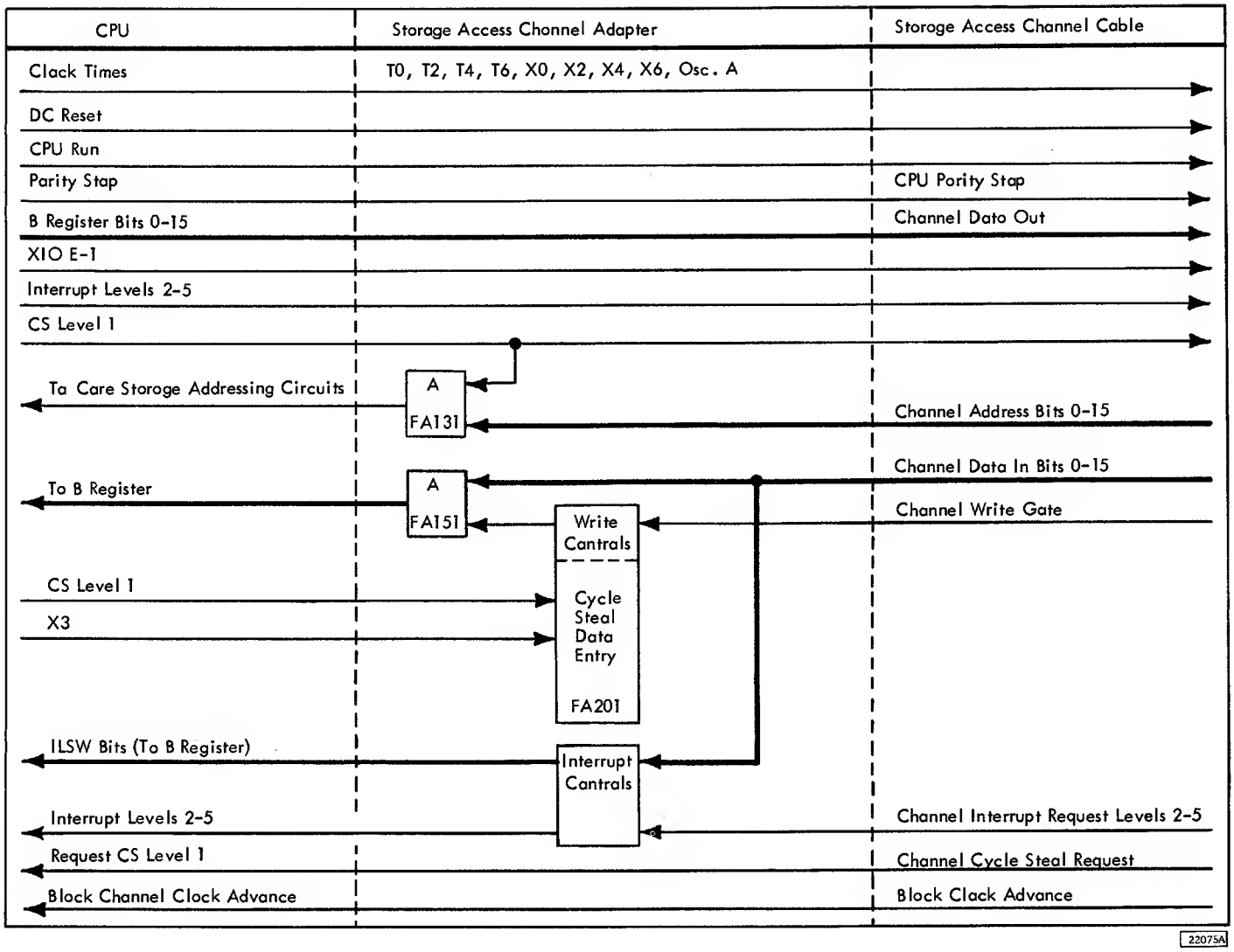


Figure 5-2. SAC Data Flow

supplied to the devices via the SAC to allow the devices to synchronize with the CPU in cycle steal operations.

DC Reset: The SAC uses this line to indicate to the devices that the CPU power sequencing is complete or that the reset key has been pressed. The reset key must also be pressed while any I/O device using the SAC is being powered down.

CPU Meter Out: The SAC uses this line to indicate to the devices that the CPU meter is running and to enable usage meters to run.

Parity Stop: The SAC uses this line to indicate to the devices that the CPU, if in parity stop mode, has detected a parity error and turned off the run controls.

CPU Clock Out: This line signals the SAC devices that the CPU T- or X-clock is running. No device should be enabled or disabled while this line is active.

B-Register Bits 0-15: These lines reflect the contents of the B-register to the devices on the SAC at all times. These lines are called 'channel data out bit (0-15)' lines to the devices. The SAC uses them to transfer instructions and data to the devices.

XIO E1: The SAC uses this line to indicate that the IOCC control word is on the 'channel data out' lines and that the devices must decode the area and func-

tion fields. The devices then must be able to keep track of E2 and E3 cycles if these cycles are needed for the operation.

Interrupt Levels 2-5: These lines signal the devices on the SAC the highest interrupt level in progress so that the devices can gate the proper ILSW to the B-register.

Cycle Steal Level 1: This line in the SAC adapter gates the 'channel address bit' lines to the core storage addressing circuits. The 'CS level 1' line indicates to the devices that a level 1 CS cycle is in progress.

Inhibit Burst Mode CS Request: This line can prevent a CS request from a device if interrupt level 0 or 1 is active or has been requested. Also, a CS request from a SAC device can be blocked if CS level 2 or 3 is active.

DEVICE TO CPU LINES

Channel Address Bits 0-15: These lines are gated to the core storage addressing circuits from the selected device on level 1 cycle steal cycles to address core storage.

Channel Data In Bits 0-15: These lines are gated to the B-register when transferring ILSW, DSW, or read data to the CPU.

CPU Meter In: This line signals the CPU that a device is in operation. The line is part of the control for the CPU usage meter.

Channel Write Gate: The devices use this line to control the transfer of data from the devices to the B-register.

Channel Interrupt Request Levels 2-5: Each of these four lines indicates to the CPU interrupt controls the need for service by one of the devices on the SAC.

Channel Cycle Steal Request: This line indicates to the CPU cycle steal controls the need for a level 1 CS cycle.

Block Clock Advance: The devices on SAC can use this line to stop the CPU cycle steal clock at X2 as well as the normal stopping time, X7.

Advance I/O Entry: This line allows a device to activate the channel data entry sample at X1 instead of X3 during a level 1 CS cycle.

PRINCIPLES OF OPERATION

- Execution of an XIO instruction makes the control word of the IOCC available to all devices connected to the SAC.
- Circuits of each device compare the area code in the IOCC with the assigned code of the device.
- Recognition of its area code causes the selected device to start the operation defined by the function code in the IOCC and decoded in the device circuits.
- Device itself determines which function codes and modifiers are applicable.

During the E1 cycle in execution of an XIO instruction, the B-register in the CPU is set to the control word of the addressed IOCC. At that time, each B-register flip-flop that is on activates the corresponding 'channel data out (0-15)' line. Also the 'XIO E1' line is activated to all devices on the SAC.

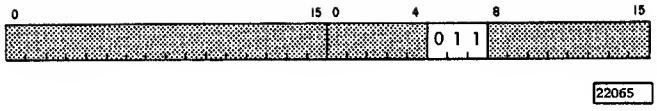
When the area code is the same as that assigned to a device that uses the SAC, the device circuits sense the fact that the device has been selected. Circuits of the selected device are set to complete execution of the function called for in the IOCC. All functions are not necessarily applicable to all devices, and the device determines which determines which function codes are to start action of the device.

The SAC and its adapter provide all the lines necessary so that any device may respond to any or all of the function codes described in the following paragraphs.

SENSE INTERRUPT (011)

- No area code required.
- ILSW for the active interrupt level is set into the CPU accumulator, via the B-register.

The IOCC that is in the B-register during the E1 cycle is:



No area code is set in the IOCC, because it is not known. The objective of the instruction is to set the ILSW into the accumulator so that the program can determine which device caused the interrupt level presently active.

If a device, assigned to the presently active interrupt level, has requested the interrupt, the device activates its assigned 'channel data in' line. During the E2 cycle, the device activates the 'channel write gate' line and, in turn, the 'channel data entry gate.' The latter line gates the active 'channel data in' line to activate the corresponding line in the I/O bus. CPU circuits then set the bit in the B-register and transfer it to the accumulator. The timing is shown in Figure 5-3.

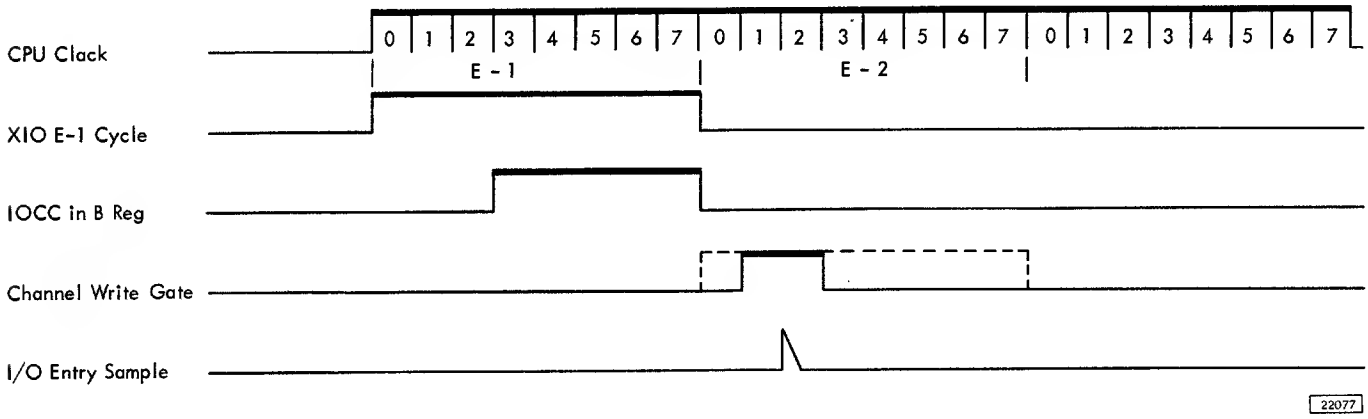
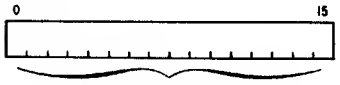


Figure 5-3. Timing for XIO Sense ILSW and Sense DSW

Depending on the system configuration, the ILSW could be any one of the following examples. As previously described, the SAC device can be assigned to level 2, 3, 4, or 5 by the user.

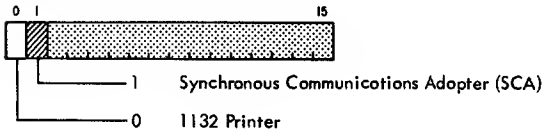
Interrupt Level Status Word - Level 0



The 1442 is the only device that interrupts on level 0. There is no ILSW bit for level 0.

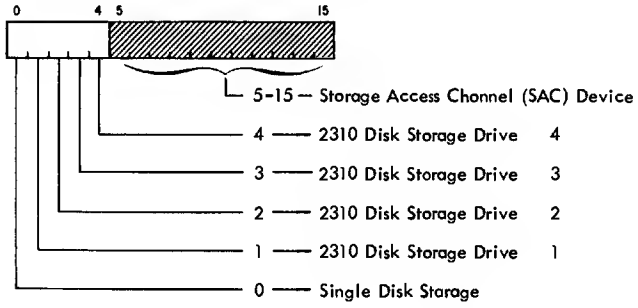
8R0280

Interrupt Level Status Word - Level 1



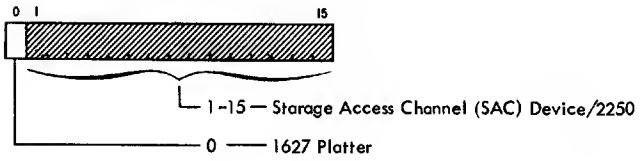
8R0281

Interrupt Level Status Word - Level 2



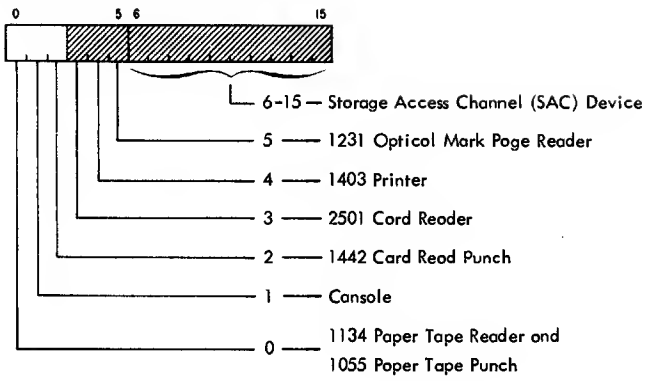
8R0282

Interrupt Level Status Word - Level 3



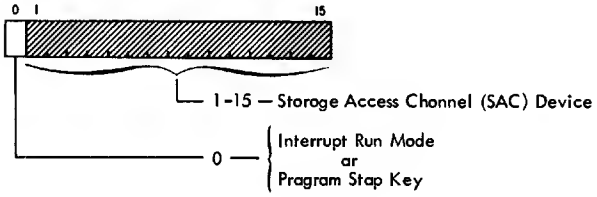
8R0283

Interrupt Level Status Word - Level 4



8R0284

Interrupt Level Status Word - Level 5



8R0285

Legend:

Not used.

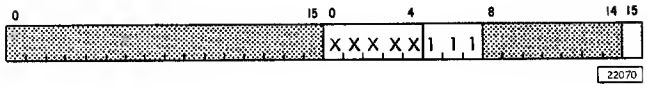
Used on B level machines only.

Used on A and B level machines. Levels 1, 2, 3 and 5 do not require on ILSW bit on A level machines. Level 0 does not require on ILSW bit on either level machine.

SENSE DEVICE (111)

- Device circuits decode the area and function codes.
- DSW for the selected device is set into the CPU accumulator, via the B-register.

The IOCC that is in the B-register during the E1 cycle is:



When a device senses its own area code and the sense device function on the 'channel data out' lines, status conditions within the device activate 'channel data in' lines. In other words, at this time, the 'channel data in' lines represent the DSW. The status conditions which activate DSW bits depend on the device circuits; e.g., write response, read response, and error.

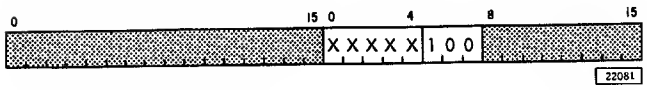
While the 'channel data in' lines are active, the device activates the 'channel write gate.' In turn, the 'channel data entry gate' is activated. The latter line gates all the 'channel data in' lines, allowing them to activate the corresponding lines in the I/O bus. CPU circuits then set the B-register with the DSW, and the DSW is later transferred to the accumulator. This timing is shown in Figure 5-3.

Status conditions in the device that cause interrupt requests can be turned off by setting the modifier bit 15 to one. If the device interrupts on more than one level, the conditions are turned off by modifier bit 15 for the highest level, bit 14 for the next highest level, etc. The device circuits must provide this XIO sense reset function.

CONTROL (100)

- Control function usually starts mechanical action in the selected device.
- Modifier bits and address word can be used for additional definition of the function to be performed.

The IOCC that is in the B-register during the E1 cycle is:



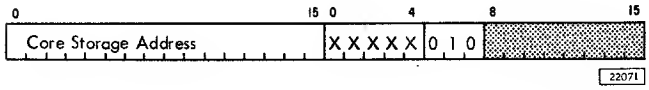
By the end of the E1 cycle, some SAC devices are completely set to perform the function called for. Any modifier bits are available on the channel data out bus. In these cases, the CPU E2 cycle taken has no effect.

For some SAC devices, further definition of the function is required. During the E2 cycle, the address word of the IOCC is set into the B-register, where it is available to the device via the channel data out bus. The device circuits can use such bits as are necessary to perform the control function.

READ (010)

- Read function usually causes transfer of one data word from a SAC device to core storage.
- Device circuits must recognize times in the CPU E3 cycle.

The IOCC that is in the B-register during the E1 cycle is:



The 'XIO E1' line to the devices on the SAC causes the devices to decode the area and function codes. The selected device sets up controls to take an E2 cycle (Figure 5-4).

E2 Cycle: The CPU sets the address word of the IOCC in the accumulator. This word is the core storage address where the data word is to be stored. The device sets up controls to take an E3 cycle.

E3 Cycle: The device activates the lines of the channel data in bus corresponding to the data to be transferred. 'Channel write gate' is activated by the device, and this line activates the 'channel data entry gate' line. The latter line gates the channel data in lines to the B-register, and the CPU writes the word into core storage.

WRITE (001)

- Write function usually causes transfer of one data word from core storage to a SAC device.
- Device circuits must recognize a CPU E3 cycle in order to store the data word in the device during that cycle.

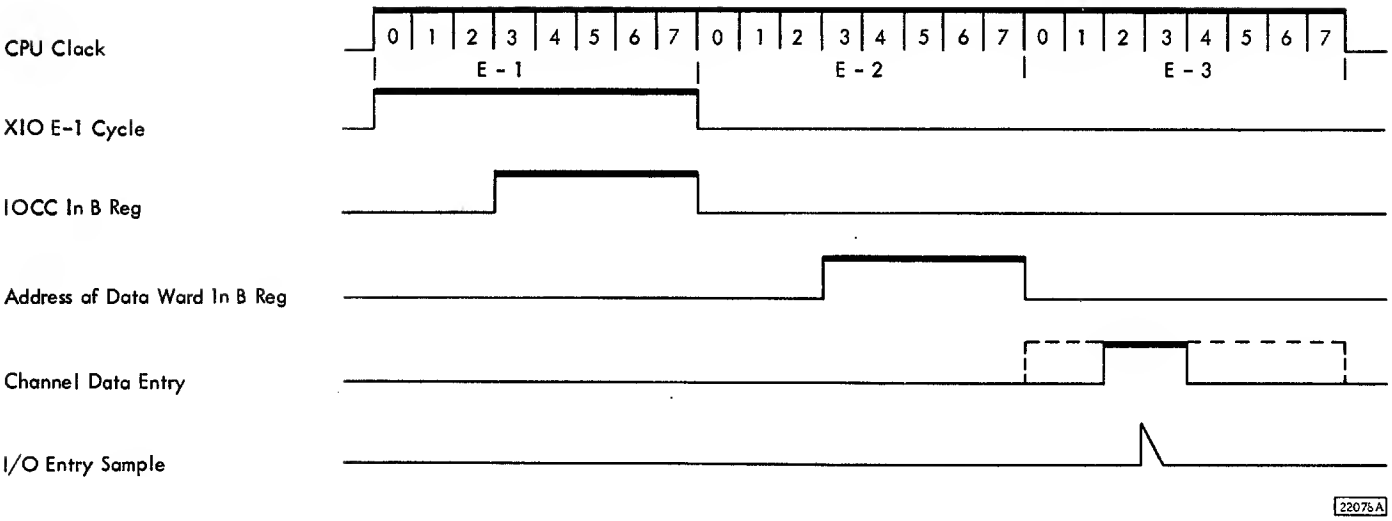
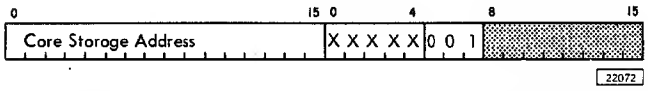


Figure 5-4. Timing for XIO Read

The IOCC set into the B-register during the E1 cycle is:



The 'XIO E1' line to the devices on the SAC causes the devices to decode the area and function fields. The selected device sets up controls to take an E2 cycle.

E2 Cycle: The CPU sets the address word of the IOCC in the accumulator. This word is the core storage address where the data word is stored. The device sets up controls to take an E3 cycle.

E3 Cycle: By T2 of the E3 cycle, the B-register is set with the data from the core storage location selected by the address word of the IOCC. The corresponding 'channel data out bit (0-15)' lines are active. At that time, the device circuits must store the data to be used by the device.

INITIATE READ (110)

- Initiate read function is usually used with a SAC device that transfers data in the cycle steal (CS) mode.
- First word of the data table used contains a word count.
- Address word of the IOCC contains the core storage address of the word count (WCA).
- Device must contain a CS address register to address core storage.

The IOCC for an 'initiate read' function and the usual format of the data table are shown in Figure 5-5.

The XIO El line to the devices on the SAC causes the devices to decode the area and function codes. The selected device sets up controls to take an E2 cycle (Figure 5-6).

E2 Cycle: The device circuits set the WCA into the device CS address register from the channel data out bus. During the E1 and E2 cycles, control circuits in the device are set up so that the device can request CS cycles for data transfers.

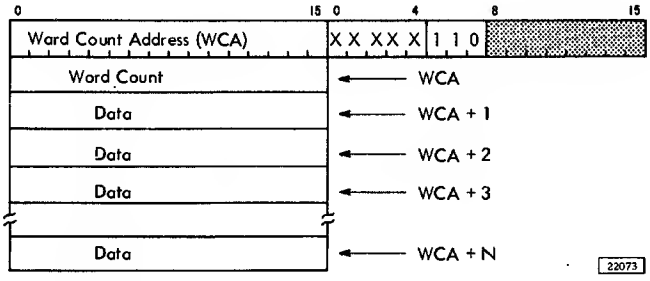


Figure 5-5. IOCC and Data Table (Initiate Read)

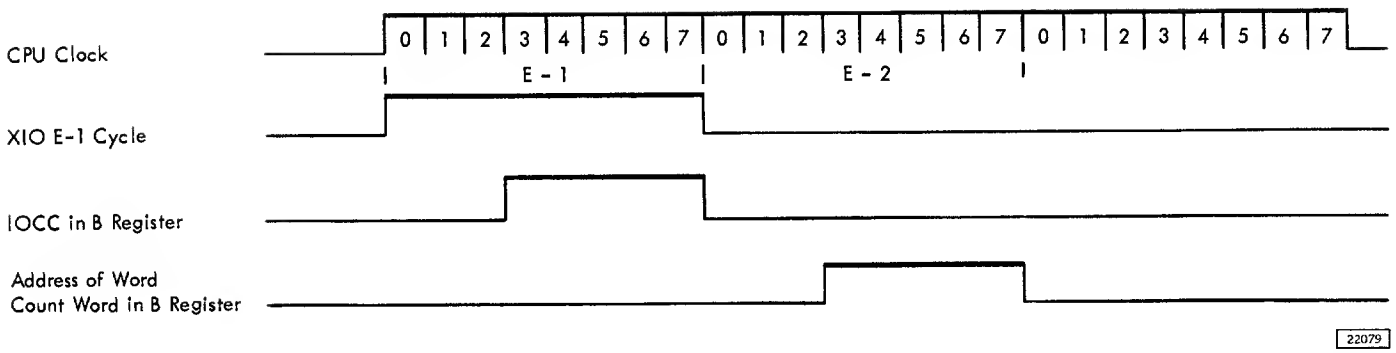


Figure 5-6. Timing for XIO Initiate Read or Initiate Write

After the E2 cycle, the CPU can go on to the next instruction unless the device signals an immediate CS request. Any device on the SAC and operating in CS mode uses CS level 1.

Cycle Steal Cycles: The first CS cycle transfers the word count to the device circuits. In the first CS cycle, the device CS address register contains the WCA and activates the corresponding 'channel address bit' lines. 'CS level 1' gates these lines to the core storage addressing circuits in the CPU. The word count is set into the B-register and transferred to the device circuits, via the channel data out bus. Device circuits step the address in the CS address register, so that the next core location is addressed during the next CS cycle.

The word count is used by the device circuits to determine the number of data transfer CS cycles to follow. Each time a data word is ready in the device, the device, the device activates the 'channel CS request' line. Unless the 'CPU stop latch' line from the CPU is active, the SAC adapter activates the 'request CS level 1.' Figure 5-7 shows timings for the data transfer CS cycles.

The 'CS level 1' line is active during each data transfer CS cycle. This line gates the address from the CS address register to the core storage addressing circuits. The device sets the data word on the 'channel data bit' lines and activates the channel write gate line (Figure 5-8). The data is gated to the B register and written into core storage.

The CPU continues with the program and the device reads the next word.

The read, cycle steal sequence continues until the number of words specified by the word count has been transferred.

INITIATE WRITE

- Initiate write function is usually used with a SAC device that transfers data in the cycle steal (CS) mode.
- First word of the data table used contains a word count.
- Address word of the IOCC contains the core storage address of the word count (WCA).
- Device must contain a CS address register to address core storage.

The IOCC for an initiate write function and the usual format of the data table are shown in Figure 5-9.

The 'XIO E1' line to the devices on the SAC causes the devices to decode the area and function codes. The selected device sets up controls to take an E2 cycle (Figure 5-6).

E2 Cycle: The device circuits set the WCA into the device CS address register from the channel data out bus. During the E1 and E2 cycles, control circuits in the device are set up so that the device can request CS cycles for data transfers.

After the E2 cycle, the CPU can go on to the next instruction unless the device signals an immediate CS request. Any device on the SAC operating in CS mode uses CS level 1.

Cycle Steal Cycles: The first CS cycle transfers the word count to the device circuits. In the first CS cycle, the device CS address register contains

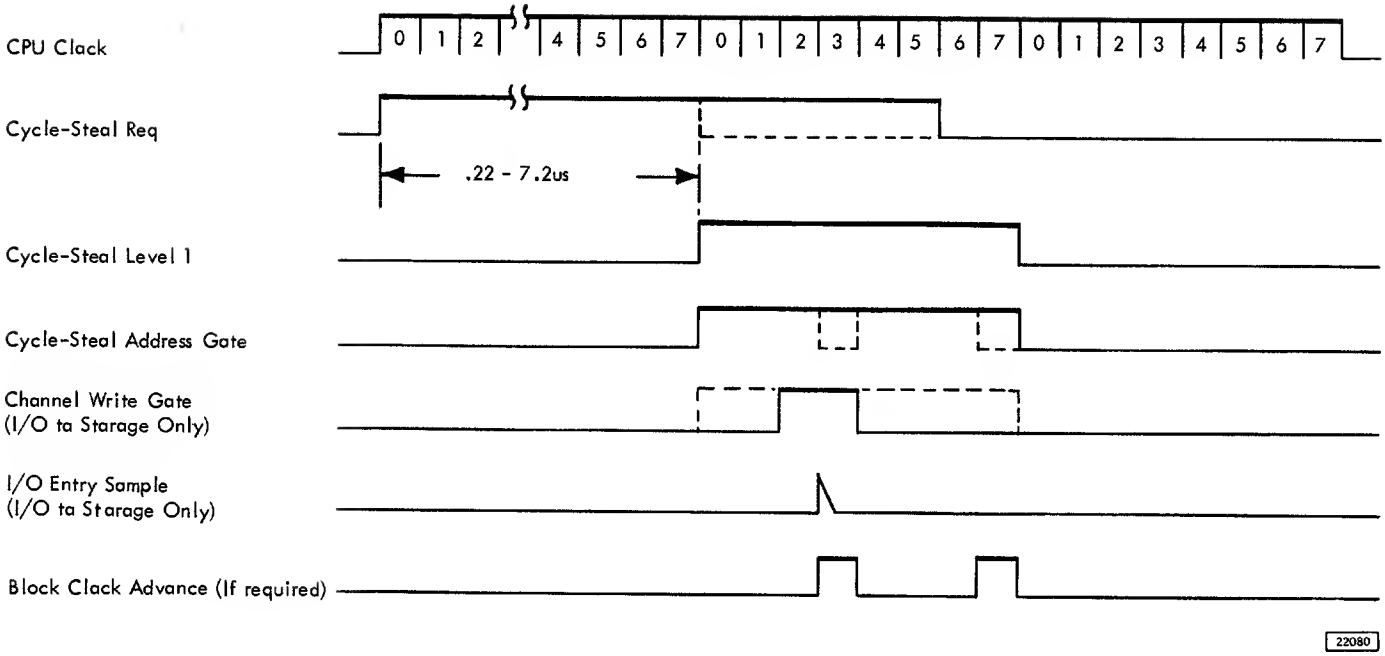


Figure 5-7. Timing for Cycle Steal Cycles

the WCA and activates the corresponding 'channel address bit' lines. 'CS level 1' gates these lines to the core storage addressing circuits in the CPU. The word count is set into the B-register and transferred to the device circuits via the channel data out bus. Device circuits step the address in the CS address register, so that the next core location is addressed during the next CS cycle.

The word count is used by the device circuits to determine the number of data transfer CS cycles to follow. The second CS cycle in a write operation is usually requested by the device immediately following the transfer of the word count. The device CS address register is gated to address core storage and the first data word is set into the B-register. The device circuits must set a "write" buffer with the data word, available to it on the channel data out bus.

The CPU continues with the program, and the device writes the data word.

The write, cycle steal sequence continues until the number of words specified by the word count has been transferred.

FEATURES

There are no features for the IBM storage access channel adapter.

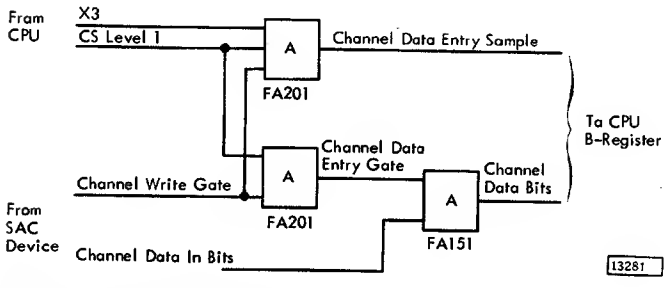


Figure 5-8. Cycle Steal Data Transfer

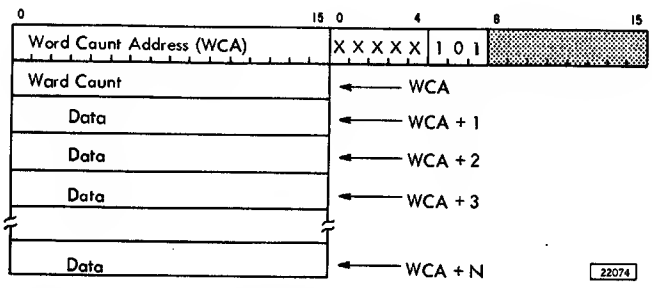


Figure 5-9. IOCC and Data Table (Initiate Write)

POWER SUPPLIES AND CONTROL

Power for the IBM storage access channel adapter is provided and controlled by the CPU.

CONSOLE AND MAINTENANCE FEATURES

There are no console and maintenance features in the IBM storage access channel adapter.

INTRODUCTION

FUNCTIONS OF THE SYNCHRONOUS COMMUNICATIONS ADAPTER

- Adapter circuits are contained in the 1131 Central Processing Unit (CPU).
- Communications line signals are presented to the adapter circuits through various types of data communications equipment.
- The synchronous communications adapter can operate in synchronous transmit-receive (STR) mode or in binary synchronous communications (BSC) mode.
- The communications adapter is under program control, operating on an interrupt level basis similar to other input/output (I/O) devices of the 1130 system.

The IBM 1130 Computing System synchronous communications adapter (SCA) provides the 1130 system with the ability to communicate with other systems and machines. Communication may be in the synchronous transmit-receive (STR) mode or the binary synchronous communications (BSC) mode. Either private or commercial common-carrier communications facilities may be used. All communications adapter circuits are contained within the 1131 Central Processing Unit (CPU) of the IBM 1130 system. Transfer of signals between the adapter circuits and the communication lines is through a data set.

Data is transferred to or from the adapter one complete character at a time, and is transmitted or received serially by bit. Characters are transmitted or received continuously, with no start or stop bits required to separate characters. Either data terminal (D/T) or data set (D/S) clocking can be selected by jumpers in the SCA to control the shifting of data to or from the adapter.

STR mode requires that characters be transmitted or received in standard four-of-eight code at switch selectable rates of 600, 1200, 2000, or 2400 bits per second. Bit rates are selected within the limits established by the data set to match the rate of the remote terminal. BSC mode allows characters (or frames) of six, seven, or eight bit lengths to be transmitted or received at bit rates of 600, 1200, 2000, 2400, or 4800 bits per second.

The CPU program must handle character encoding and decoding in either mode. In addition, in BSC mode, the program must handle changes of frame length.

All operations are under direct program control of the CPU. The communications adapter operates on the interrupt/request basis that is used by other input/output devices of the IBM 1130 Computing Systems. The SCA interrupts on interrupt level 1.

CONNECTIONS

- SCA circuits are connected to other circuits within the CPU by the standard interboard connectors.
- Adapter circuits are connected to the data set by a cable which contains signal ground and frame ground lines in addition to the necessary signal lines.
- Data lines (transmit and receive are normally at the "mark" level.)
- Type of data set used is largely dependent on transmission speed.
- Both STR and BSC modes operate in half-duplex, using either half-duplex (two-wire) or full-duplex (four-wire) communication lines.

Signal lines from the adapter to the data set are:

1. Data terminal ready: Signals that the adapter has received or is executing an instruction to transmit or receive, and is not in diagnostic mode. If desired, a jumper can be removed, forcing a continuous 'data terminal ready' (FC331).
2. Request to send: Signals that the adapter is transmitting in a two-wire system, or is either transmitting or receiving in a four-wire system (FC361).
3. Transmit data: Determines by its voltage level whether the data is a 1 (mark) or a 0 (space). A down level (-) is a mark level, and an up level (+) is a space level at the data set interface (FC361).
4. Transmit timing provides timing from the adapter circuits (internal clocking) for transmit operations.

Signal lines from the data set to the adapter circuits, shown on FC361, are:

1. Data set ready: Answers a data terminal ready signal when power is on the data set and all necessary connections are established.
2. Clear to send: Signals that the data set can start a transmit operation. This signal becomes active approximately 200 ms after a request to send from the adapter, and remains active as long as request to send remains active. The delay is a function of the data set.
3. Ring indicator: Signals that the data set has received a ring signal from the communications lines.
4. Receive data: Determines by its voltage level whether the receive data bit is a 1 or a 0.
5. External transmit timing: Controls the shifting of data from the transmit serializer register. This line is used only when the adapter is set up for data set (D/S) clocking.
6. Receive timing: Controls the shifting of data into the receive deserializer register when the adapter is using data set (D/S) clocking.

When no transmit or receive operation is in progress, the 'transmit data' and 'receive data' lines are at the mark level. A change from this level to the space level or from the space level back to the mark level is called a transition.

The data set cable has a multiple switch, which may be set to either TEST or OPERATE. With the switch set to TEST, certain signals from the adapter to the data set are returned to the adapter without entering the data set (FC001). This allows the adapter to run tests without the data set.

The data set used in the United States for connecting the adapter to the private or commercial communications lines is defined by Electronics Industries Association (EIA) Standard RS-232-B. Outside the United States, the data set used is defined by the Consultive Committee on International Telephone and Telegraph (CCITT) Standard. Of the facilities meeting the standards, the particular data set and type of service selected depends on the baud (bit rate or speed) which is required to match the capability of the remote terminal.

Additional information on Teleprocessing and data sets may be found in Introduction to Teleprocessing (Z25-2522)* and Common Carrier Facilities for Teleprocessing (Z25-2529).*

*IBM Confidential, for release only to authorized persons.

Half-Duplex and Full-Duplex Operations

Half-duplex operation allows either terminal to transmit or receive data, but neither terminal can do both simultaneously. Communication proceeds with each terminal alternately transmitting and receiving data, similar to a telephone conversation.

Full-duplex operation for the SCA allows either terminal to transmit or receive non-data (idle) characters on one set of wires while receiving or transmitting data on the other set of wires. This is as close to full-duplex as can be accomplished by the SCA -- the transfer of data between terminals, and to or from the CPU, is still in half-duplex because only one data buffer exists in the adapter.

Half-Duplex (Two-Wire) Operation

Synchronous transmit-receive or binary synchronous operation with a two-wire half-duplex system requires a delay of approximately 200 milliseconds when the terminal starts to transmit. This 'clear to send' delay, also called turnaround delay, allows the data set and the communications lines to reverse the direction of transmission and line echo to settle. The amount of delay is therefore related to the character of the line and data set. Turnaround delay is a function of the data set. When this delay is completed, the data set signals the adapter. The adapter does not transmit until the data set signals 'clear to send' at the completion of the turnaround delay. Once activated, 'clear to send' remains active as long as 'request to send remains active.

Two jumpers must be installed for half-duplex (two-wire) operation. One controls activating of 'request to send,' and consequently 'clear to send' (FC361). The other jumper (FC131) allows locking the transmit clock to the receive clock.

Full-Duplex (Four-Wire) Operation

When the adapter is connected to a four-wire full-duplex system, the 200-ms turnaround delay is eliminated, because no delay is required for line echo to die down. For full-duplex operation, the half-duplex jumper is removed (FC361) and the full-duplex jumper added (FC331). 'Request to send' and 'clear to send' then remain active all the time.

In STR mode of operation, the adapter remains synchronized by repeatedly transmitting some known non-data (idle) character on one pair of wires while receiving data on the second pair of wires. Note that this type of operation is as near full-duplex as can be accomplished by the SCA.

In the BSC mode of operation, resynchronization of the receiving terminal to the transmitting terminal is always necessary when a new transmission is started. Synchronization occurs when the receiving terminal recognizes two consecutive characters like the character in the idle-sync register.

The half-duplex jumper (FC131) set for full-duplex prevents locking the transmit clock to the receive clock while operating in STR mode. This allows the receive clock to adjust to incoming bits while data is being transmitted on the other pair of lines. BSC mode allows locking the clocks in either half-duplex (two-wire) or full-duplex (four-wire) operation when using data terminal (D/T) clocking.

Graphic	4 of 8 Code	
	N X O R	8 4 2 1
blank	1 1 1 1	0 0 0 0
¢	0 1 1 0	1 0 1 0
.	1 0 0 0	1 0 1 1
<	0 1 1 0	1 1 0 0
(	0 1 0 1	0 1 1 0
+	0 0 1 1	0 1 1 0
!	1 0 0 0	1 1 0 1
&	1 0 0 0	1 1 1 0
!	1 1 0 0	1 0 1 0
$	0 1 0 0	1 0 1 1
*	1 1 0 0	1 1 0 0
)	0 1 0 1	1 1 0 0
;	0 0 1 1	1 1 0 0
¬	0 1 0 0	1 1 0 1
-	0 1 0 0	1 1 1 0
/	1 0 1 1	0 0 0 1
,	0 0 1 0	1 0 1 1
%	1 0 1 0	1 1 0 0
_	0 1 0 1	1 0 1 0
>	0 0 1 1	1 0 1 0
?	0 0 1 0	1 1 0 1
:	0 0 1 0	1 1 1 0
#	0 0 0 1	1 0 1 1
@	1 0 0 1	1 1 0 0
'	0 0 0 0	1 1 1 1
=	0 0 0 1	1 1 1 0
"	0 0 0 1	1 1 0 1
A	0 1 1 1	0 0 0 1
B	0 1 1 1	0 0 1 0
C	0 1 1 0	0 0 1 1
D	0 1 1 1	0 1 0 0
E	0 1 1 0	0 1 0 1

Graphic	4 of 8 Code	
	N X O R	8 4 2 1
F	0 1 1 0	0 1 1 0
G	1 0 0 0	0 1 1 1
H	0 1 1 1	1 0 0 0
I	0 1 1 0	1 0 0 1
J	1 1 0 1	0 0 0 1
K	1 1 0 1	0 0 1 0
L	1 1 0 0	0 0 1 1
M	1 1 0 1	0 1 0 0
N	1 1 0 0	0 1 0 1
O	1 1 0 0	0 1 1 0
P	0 1 0 0	0 1 1 1
Q	1 1 0 1	1 0 0 0
R	1 1 0 0	1 0 0 1
none	1 0 1 0	1 0 1 0
S	1 0 1 1	0 0 1 0
T	1 0 1 0	0 0 1 1
U	1 0 1 1	0 1 0 0
V	1 0 1 0	0 1 0 1
W	1 0 1 0	0 1 1 0
X	0 0 1 0	0 1 1 1
Y	1 0 1 1	1 0 0 0
Z	1 0 1 0	1 0 0 1
0	1 0 0 1	1 0 1 0
1	1 1 1 0	0 0 0 1
2	1 1 1 0	0 0 1 0
3	1 0 0 1	0 0 1 1
4	1 1 1 0	0 1 0 0
5	1 0 0 1	0 1 0 1
6	1 0 0 1	0 1 1 0
7	0 0 0 1	0 1 1 1
8	1 1 1 0	1 0 0 0
9	1 0 0 1	1 0 0 1

11470

Figure 6-1. 4- of -8 Transmission Code

MODES OF OPERATION

- Toggle switch setting determines which mode of operation can be performed -- STR or BSC.
- Different programs are required for the two modes.

The mode of operation is determined by the setting of a toggle switch and may be either synchronous transmit-receive (STR) or binary synchronous communications (BSC). Because all operations of the adapter are under direct program control of the CPU, different programs are required for each mode. Only a general description of the the two modes of operation can be given, because the programs can vary considerably. Data and control characters for SCA operations must appear in bit positions 0 through 7 of the CPU B-register, to be transferred to the SCA circuits.

Synchronous Transmit-Receive

- STR mode operates only in a point-to-point communications system.
- Character coding is restricted.

The synchronous transmit receive mode of operation allows the adapter to function only in a point-to-point system; i.e., only connected to a single remote terminal at any time. Character coding is restricted to a fixed-count four-of-eight code, consisting of 64 data characters (Figure 6-1) and six control characters, which are never used as data characters. Two characters are used as data or control characters, depending on when they appear.

Control characters are transmitted in control sequences, each of which has a leader character and a trailer character. The leader character may be a transmit leader (TL), a control leader (CL), or a group mark (GM), and is an indication that a control sequence is being entered. When the SCA receives a control sequence, the CPU program must analyze the characters to determine the next function of the terminal. Control characters are shown in Figure 6-2, and control sequences are shown in Figure 6-3. For all characters the N, X, O, R, 8, 4, 2, and 1-bit positions shown are stored in CPU storage word bit positions 0 through 7, respectively.

Control Chorocters	4 of 8 Code							
	N	X	O	R	8	4	2	1
Idle	0	0	1	1	1	0	0	1
Start of Record 1 or Acknowledge 1 (SOR 1 or ACK 1)	0	1	0	1	0	0	1	1
Start of Record 2 or Acknowledge 2 (SOR 2 or ACK 2)	0	0	1	1	0	0	1	1
Tronsmit Leader (TL)	0	0	1	1	0	1	0	1
Control Leader (CL)	0	1	0	1	0	1	0	1
End of Transmission (EOT) *	0	1	0	1	1	0	1	0
Inquiry or Error (INQ or ERR)	0	1	0	1	1	0	0	1
Telephone *	0	1	0	1	1	1	0	0
Longitudinal Redundancy Check (LRC) **	-	-	-	-	-	-	-	-

* Also used as o dato chorocter

** The LRC character contoins a 1 in each bit position for which the total of 1's in the record was odd, ond a 0 if the total wos even. The chorocter is not necessorily in the 4 of 8 code.

13121

Figure 6-2. Control Characters

Control Sequence	Control Character Sequence	
	Leader Character	Trailer Character
End of IDLE (EOI)*	CL	1 IDLE
Inquiry (Synchronized ?)*	TL	INQ
Acknowledge (Synchronized)	CL	ACK 2
Telephone Sequence *	CL	TEL
Acknowledge Telephone *	CL	TEL
Start of Record 1 (SOR 1) 1st or odd numbered record	TL	SOR 1
Start of Record 2 (SOR 2) 2nd or even numbered record	TL	SOR 2
End of Transmittol Record (EOTR)	TL	LRC
Acknowledge Record 1	CL	ACK 1
Acknowledge Record 2	CL	ACK 2
Repeot Last Record (ERROR)	CL	ERR
Intermediote LRC**	GM	LRC
End of Transmission (EOT)*	CL	EOT
Acknowledge EOT *	CL	EOT

*These sequences are always preceded by a 1.25 second transmission of IDLE characters.

** This sequence may be required on some terminals i.e. 1013, 7701, 7702

16163c

Figure 6-3. Control Sequences

Example of STR Communication

In the following example of STR communication, an 1130 system with the SCA feature transmits a message to some remote STR terminal. Only the instructions necessary to illustrate the 1130 operation are shown (Figure 6-4).

When both terminals are connected to the communications lines, the next step is to establish bit and character synchronization. Both terminals attempt to send 1.25 to 1.5 seconds of idle characters (the SCA sends 1.25 seconds), followed by an end-of-idles control sequence consisting of CL and another idle. Then both terminals enter receive mode for approximately 3 seconds and attempt to receive and recognize the end-of-idles sequence from the other. As soon as either terminal recognizes one or more idles followed by the end-of-idles sequence, the two terminals go into a "handshaking" mode, in which the terminals alternate in transmitting and receiving idles. Because the programs are not being started at the same instant and because the timers vary somewhat in duration, it seldom takes long to start handshaking.

In the example (a two-wire operation), the 1130 system has a message to send. The 'start read' instruction has a 1 in bit 15 position to establish the SCA as the "master" terminal. The remote terminal must be the "slave" with its transmit clock locked to its receive clock, which, in turn, is synchronized to the SCA transmit clock. Once the SCA receive clock has been synchronized to the remote terminal's transmit clock, all clocks are effectively synchronized to the SCA transmit clock.

Handshaking may continue for an indefinite time, although the example shows only a couple of such turnarounds. At the end of a period of idles, instead of sending an end-of-idles sequence, the 1130 program sends an inquiry control sequence, consisting of a TL and an INQ. On recognizing the inquiry if the remote terminal is ready to receive, it sends an acknowledge control sequence. Note that when

CPU Instruction	SCA Operation		Remote Terminal
Synchranize	Force Transmit Mode	IDLE	IDLE Bath Terminals Try
	Send IDLEs for 1.25 Sec.	IDLE	CL to Start "Handshaking"
		IDLE	IDLE
		IDLE	Turnaround
		IDLE	Establish Bit and Character
	Timeout Interrupt	IDLE	Synchronizotion
Write	Send End af Idles	CL	Receive IDLEs ond
Write	Sequence	IDLE	End of Idles Sequence.
Start Read-Modifier 15	Turnoround		Turnaround
	Make SCA the "Master Terminal".		IDLE This Terminal is "Slave".
	Synchranize Receive Clock to Received IDLEs		IDLE Terminals are "Hand-shaking".
			IDLE Send IDLEs and End
Read			CL of Idles Sequence.
Read			IDLE
	Turnoround		Turnaraund
Synchranize	Send IDLEs far 1.25 Sec.	IDLE	Receive IDLEs "Handshaking".
	"Handshaking"	IDLE	
		IDLE	
	Timeout Interrupt	IDLE	
Write	Send Inquiry Sequence	TL	Receive Inquiry Sequence.
Write		INQ	
Stort Read	Turnaround		Turnaround
	Receive Permissian		IDLE*
Read	to Send Message		CL
Reod			ACK 2
Start Write	Turnaround		Turnaround
	Start of Record Sequence	IDLE	
Write		TL	
Write		SOR 1	
Write (Program also Generates an LRC Character)	Send Record 1	Char 1	Receive Recard 1
Write		Char 2	
Write		Char 3	
Write		⊥	
Write		⊤	
Write	Send Last Data Charocter	Char n	
Write	Send End of Transmittal	TL	
Write	Record Sequence	LRC	Compare LRC Characterr
Start Read	Tumaround		Turnaround
	Receive Acknowledgement		IDLE*
Read	of Correct Receipt of Record		CL
Read	1 by Remate Terminal		ACK 1
Start Write	Turnaround		Turnaround

CPU Instruction	SCA Operation		Remote Terminal
	Send Start of Record	IDLE	
Write	Sequence	TL	
Write		SOR 2	
Write	Send Record 2	Chor 1	
Write (Program also Generates an LRC Choracter)		Char 2	
Write		⊥	
Write		⊤	
Write		Char n	
Write	Send End of Transmittal	TL	
Write	Record Sequence	LRC	Campare LRC Charocter
Start Read	Turnoround		Turnaround
			IDLE* (Sends Error Messoge
Read	Receive Error Indication		CL (Becouse LRC Character
Read			ERR (Gave Unequal Compare)
Start Write	Turnaround		Turnaround
	Send Start of Record	IDLE	
Write	Sequence	TL	
Write		SOR 2	
Write	Re-Tronsmit Record 2	Char 1	
Write (Program also Generates an LRC Character)		Chor 2	
Write		⊥	
Write		⊤	
Write		Char n	
Write	Send End af Tronsmittal	TL	
Write	Recard Sequence	LRC	Compore LRC Character
Start Read	Turnoround		Turnoround
	Receive Acknowledgement		IDLE*
Read	of Correct Receiptaf Record		CL
Read	2 by Remate Terminal		ACK 2
Start Write	Turnaround		Turnaround
	Send End of Transmission	IDLE	
Write	Sequence	CL	
Write		EOT	
Start Read	Turnaround		Turnaround
	Receive Acknowledgement		IDLE*
Read	of End of Transmissian		CL
Read	Sequence		EOT

Further Operation Entirely Progrom- Dependent in an SCA. Other STR Terminals Require Manual Intervention Now.

* These IDLEs may appear or nat, depending an data set and terminal.

7512?B

Figure 6-4. Typical STR Sequence

the remote terminal is an 1130, one idle precedes the CL and ACK2 sequence, although some STR terminals do not provide this idle. The program in the transmitting terminal must be capable of recognizing the acknowledge sequence with or without the preceding idle.

Transmission of the message, which may contain several records, can now start. The remote terminal must acknowledge the receipt of each record before the SCA sends another record. Each record the SCA sends starts with a start of record (SOR) sequence, consisting of a TL and either an SOR1 or an SOR2. SOR1 precedes the 1st, 3rd, and all odd-numbered records, and SOR2 precedes all even-numbered records. Note that the TL character is preceded by an automatic idle character when the SCA is transmitting. The reason is that, at the time of the first write response interrupt, the SCA buffer register has not yet been loaded by the program. Then the program transfers the SOR sequence characters, followed by the data record characters at succeeding write response interrupts.

As the record is being transmitted the program generates a longitudinal redundancy check (LRC) character. Each character, as it is presented to the SCA for transmission, is ORed with the word in some core storage location. This process continues until the end of the record, at which time the SCA sends an end-of-transmittal-record (EOTR) sequence. The EOTR sequence consists of a TL and the LRC character. The resultant LRC character contains a 1 in each position in which the whole record contains an odd number of 1's.

The remote terminal also generates an LRC character for the record being received. Then, when the remote terminal receives the EOTR sequence, the two LRC characters are compared in the remote terminal. If they are equal, the acknowledge control sequence of CL and ACK1 or ACK2 is returned to the "master" terminal. ACK1 is used for all odd numbered records, and ACK2 for all even-numbered records. This procedure ensures that the remote terminal has recognized all records.

When an unequal comparison of LRC characters occurs, an error is indicated, and the remote terminal returns a received error sequence of CL and ERR. When the CPU program recognizes the error sequence, usually one or more retransmissions are programmed before an error is indicated and manual or error recovery program intervention is requested.

The SCA sends the end of transmission (EOT) control sequence when all records of the message have been sent and all acknowledgments received. The EOT is a sequence of CL and EOT and is acknowledged by the remote terminal returning the same sequence. At this time, the program determines whether the terminals should return to handshaking, continue with other operations, or stop.

The telephone control sequence, a CL followed by a telephone (TEL) character indicates that the operator of the terminal sending the sequence desires voice communication with the operator of the receiving terminal. When the receiving terminal is an SCA, the program may decode this sequence and turn on the alarm, gain the operator's attention by a printout, or both.

The example shows that in the SCA all translation of data and control codes and generation of LRC characters are up to the CPU program. In other STR equipment, these functions may be accomplished by machine circuits. When the SCA is communicating with some STR terminal other than another 1130 system, the CPU program must be capable of recognizing differences in operation. A difference which has not been mentioned is that some STR terminals use a group mark (GM) character to indicate the end of a smaller block of data than the previously defined transmittal record. Following the group mark is the LRC character for this smaller block of data, and the receiving terminal can check each block. However, no acknowledgment is sent to the transmitting terminal until the EOTR sequence is received.

Additional information on other types of STR terminals may be found in IBM Field Engineering Manual of Instruction, Synchronous Transmitter-Receiver, Models 1 and 2 (223-6953). Additional information on SCA operation in STR mode may be found in IBM 1130 Functional Characteristics (A26-5881).

Special Programming

Special programming techniques are required in STR when an 1130 is used to communicate with certain other STR devices, such as a 1013, 1009, or 7702, and when that device is using either a 201 Data Set or an IBM 3977 Modem in two-wire operation. These data sets do not allow transmission of data or control characters prior to the clear to send signal from the data set. Therefore, no idles are

received from these devices before the control leader (CL) or transmit leader (TL). Since the 1130 SCA requires at least one recognizable character before interrupting the CPU, the following special technique should be used:

1. If the 1130 is the "slave," it is receiving records. After writing the acknowledgment character (ACK1, AKC2, or ERR), the program should load the idle-sync register with the TL. Because the TL is now the recognizable character, when it is received, it is not loaded into the buffer for the CPU to read. The first character which interrupts the CPU is the trailer. The program must indicate to itself that the TL has already been received. This should be done when the first read interrupt occurs. If the 1130 times out, the remote station may send a message beginning with a TL or it may begin "handshaking" beginning with an idle character. To cope with either possibility, after a time-out, the 1130 program loads the idle-sync register with a TL, and if another time-out occurs, the register is then loaded with an idle character. Once character phase is reestablished, the alternating of TL or idle characters ceases.
2. If the 1130 is the "master," it is sending records. After writing an INQ or the LRC character of an EOTR, the program should load the idle-sync register with the CL. Since the CL is now the recognizable character, when it is received, it is not loaded into the buffer for the CPU to read. The first character which interrupts the CPU is the trailer. The program must indicate to itself that the CL has already been received. This should be done when the first read interrupt occurs.

For both cases, the idle-sync register should be reloaded with the idle character prior to each transmission. An idle character should also remain in the idle-sync register after the program writes the idle of an end of idles sequence, or the TEL character or the EOT character of their respective sequences.

Because these techniques work for all data sets and STR devices, it is recommended that they be used wherever a mixture of data sets and/or STR devices are used. The IBM-supplied STR program uses these techniques.

Binary Synchronous Communications

- BSC mode can operate in either a point-to-point system or a multipoint system.
- Character coding is practically unrestricted.
- Major difference from STR is the method of synchronizing the units involved in the communication.

The BSC mode of operation, unlike STR, allows the communications adapter to function in either a point-to-point system or a multipoint system (connected to two or more remote terminals at one time). Transmitted data is not restricted to the eight-bit code required by the STR mode. Frame size (number of bits per character) of six, seven, or eight bits may be selected by the program.

The major difference in operation between STR and BSC modes is in synchronization between the two units which are communicating. Note that in the STR mode the terminals are synchronized by an exchange of idle characters. These idle characters are transmitted by the SCA as a result of a 'synchronize' instruction from the CPU program. Thereafter, it is not necessary to resynchronize unless communication is interrupted for more than approximately 3 seconds.

In the BSC mode of operation, synchronization is not maintained during all turnarounds. Each time a terminal starts to receive, the terminal must synchronize its internal receive clock to the incoming signals.

Sequence of Operations

As in the STR mode, the exact sequence of operations is entirely dependent upon the CPU program. The same basic procedure is followed. An inquiry routine is transmitted by a terminal to ascertain whether the remote terminal is ready to send or receive a message. The remote terminal acknowledges that it has received the inquiry. Communication then continues with the exchange of records and acknowledgments. In general, the terminal which is transmitting data determines when the communication shall end. Further descriptions of BSC operations may be found in the SRL Manual IBM 1130 Functional Characteristics (A26-5881).

PROGRAMMING

- SCA operates under direct program control of the CPU.
- Area code for the SCA is decimal 10 (01010).
- Function codes applicable to the SCA are:

  Sense interrupt
  Sense device
  Control
  Start write
  Write
  Start read
  Read

- IOCC's for each function are shown in "Principles of Operation" with the circuit descriptions.

DATA FLOW

- Data flow for transmit operations is shown in Figure 6-5.
- Data flow for receive operations is shown in Figure 6-6.
- Data flow within the adapter is shown in Figure 6-7.

Transmit (TR) Operation

When a 'start write' instruction is given by the program, and the data set is ready, an interrupt request is sent to the CPU. When interrupt priority allows it, the program branches to the interrupt level servicing subroutine which must contain a 'write' instruction. Execution of this instruction transfers a character from the CPU core storage to the SCA buffer via the B-register and the I/O bus. The character is transferred from the buffer to the transmit serializer register (TSR) when transmission of the previous character is complete.

With the adapter set for data terminal (D/T) clocking, the bits of the character are shifted through the register and presented to the data set under control of the transmit clock in the adapter circuits. With the adapter set for data set (D/S) clocking, shifting the character is accomplished by the 'external transmit timing' line from the data set. The data set converts the mark or space levels to control the signals placed on the communications lines. The operation continues until the program determines that the complete record or message has been transmitted.

Receive (RCV) Operation

A 'start read' instruction in the program conditions the SCA to receive data. Serial data from the

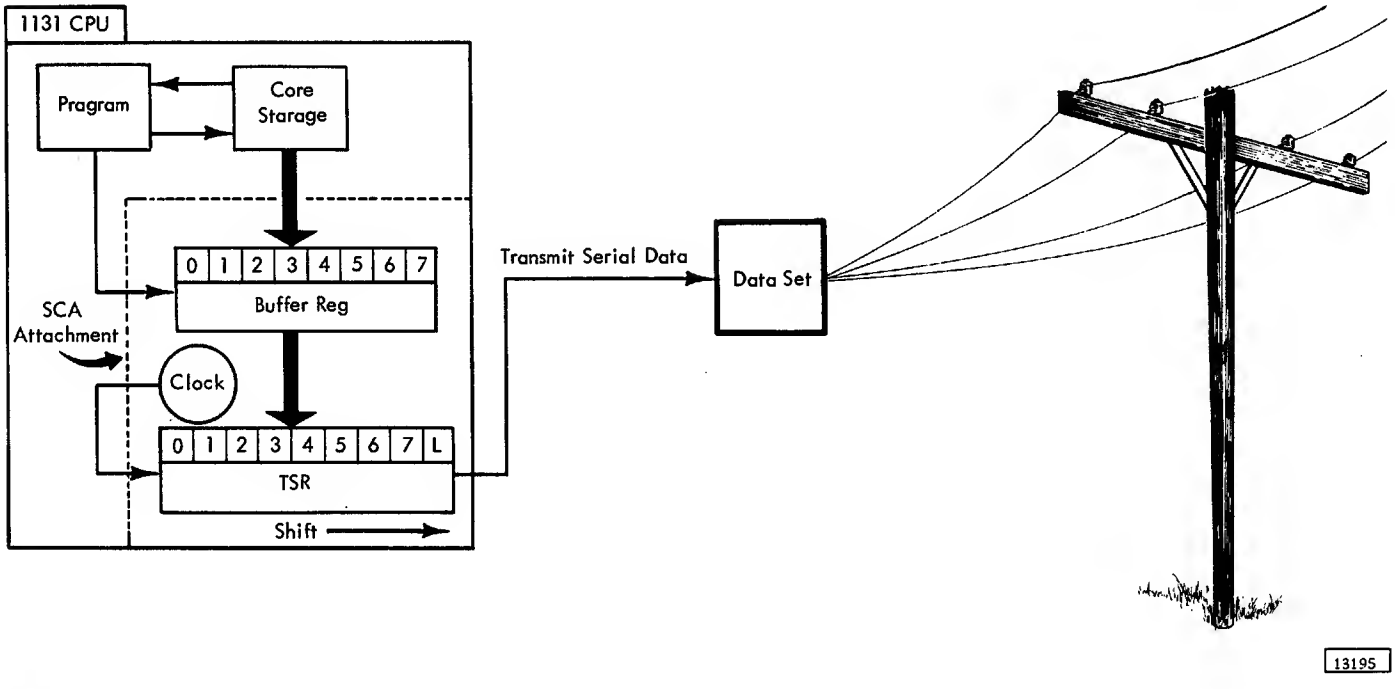


Figure 6-5. Transmit Operation

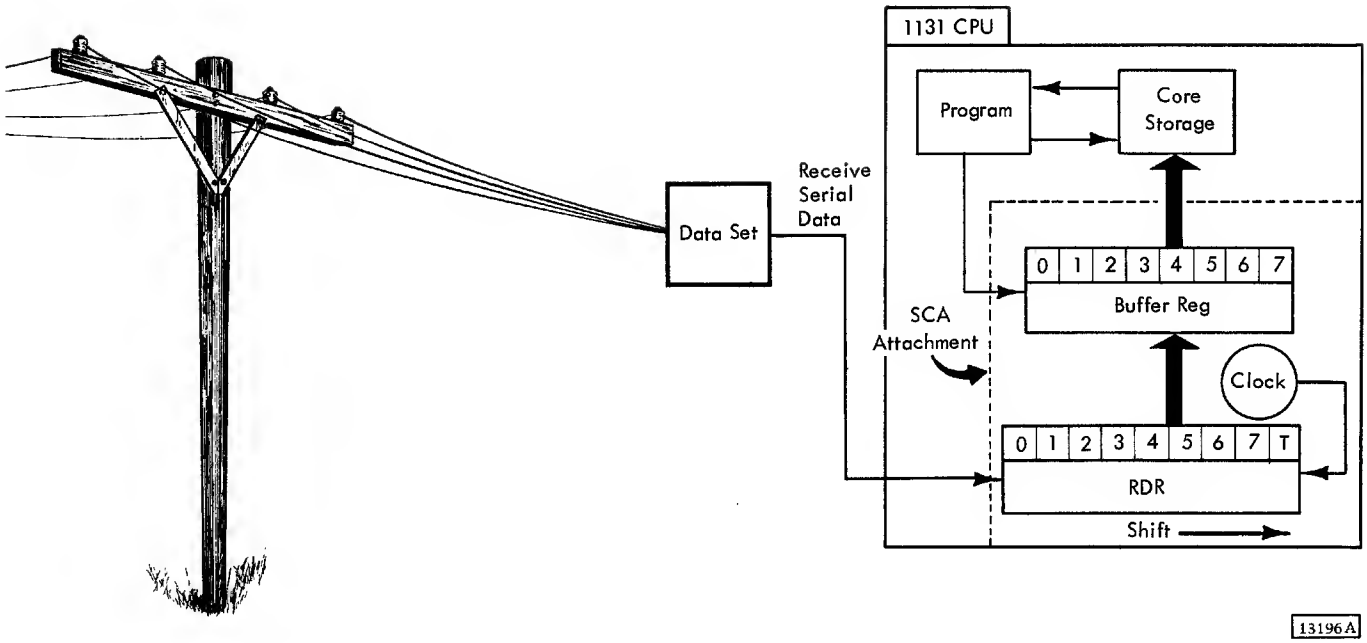


Figure 6-6. Receive Operation

communications lines, converted in the data set to mark (1) or space (0) levels, enters the receive deserializer register (RDR). Receipt of one recognizable character is all that is required in STR, while two characters are required in BSC. In STR mode, synchronization has been established during the 'handshaking" operation. In BSC mode, resynchronization is required for each receive operation. When the required one or two idle-sync characters have been recognized, and a complete non-idle character is in the RDR, the data is transferred to the buffer and an interrupt request is sent to the CPU. As soon as interrupt priority allows, the CPU program branches to a subroutine to service the interrupt. One instruction in the subroutine must be a 'read' instruction. Execution of the 'read' instruction transfers the character in the SCA buffer to the B-register via the I/O bus and writes the character in core storage. The program stops the receive operation when the turnaround control sequence is received and recognized by the program.

Diagnostic Operations

Placing the adapter in diagnostic mode, by giving a 'control' instruction with a modifier bit 12, activates the data bypass circuit. Data is transferred serially, one bit at a time, from the TSR to the RDR. The bits may be transferred from bit 6, bit 7, or the line bit position of TSR, depending on the frame length which is set. The transferred bits enter the bit 0 position of the RDR. A read response interrupt is requested each time a bit is transferred.

FUNCTIONAL UNITS

CLOCKS

- Transmit and receive clocks can be driven by either of two oscillators.
- Either data terminal (D/T) or data set (D/S) clocking can be used to control the shifting of data to and from the adapter.
- Clock operation depends on the mode of operation -- STR, BSC, or diagnostic.

The synchronous communications adapter (SCA) feature uses two clocks, a transmit clock and a receive clock (Figure 6-8). They are driven by either of two oscillators; one is 153.6 kHz and the other is 128 kHz. The 153.6-kHz oscillator, through a network of three 'frequency divider' flip-flops, provides 32 oscillator A and 32 oscillator B pulses per bit with bit rates of 600, 1200, 2400, or 4800 per second. The 128-kHz oscillator, through a single 'frequency divider' FF, provides 32 oscillator A and 32 oscillator B pulses per bit with a bit rate of 2000 per second. Clock drive pulses (Figure 6-9) are active only when the 'clock gate' FL is on, and the rate is determined by setting a rotary switch. With gated oscillator A pulses available, both clocks run.

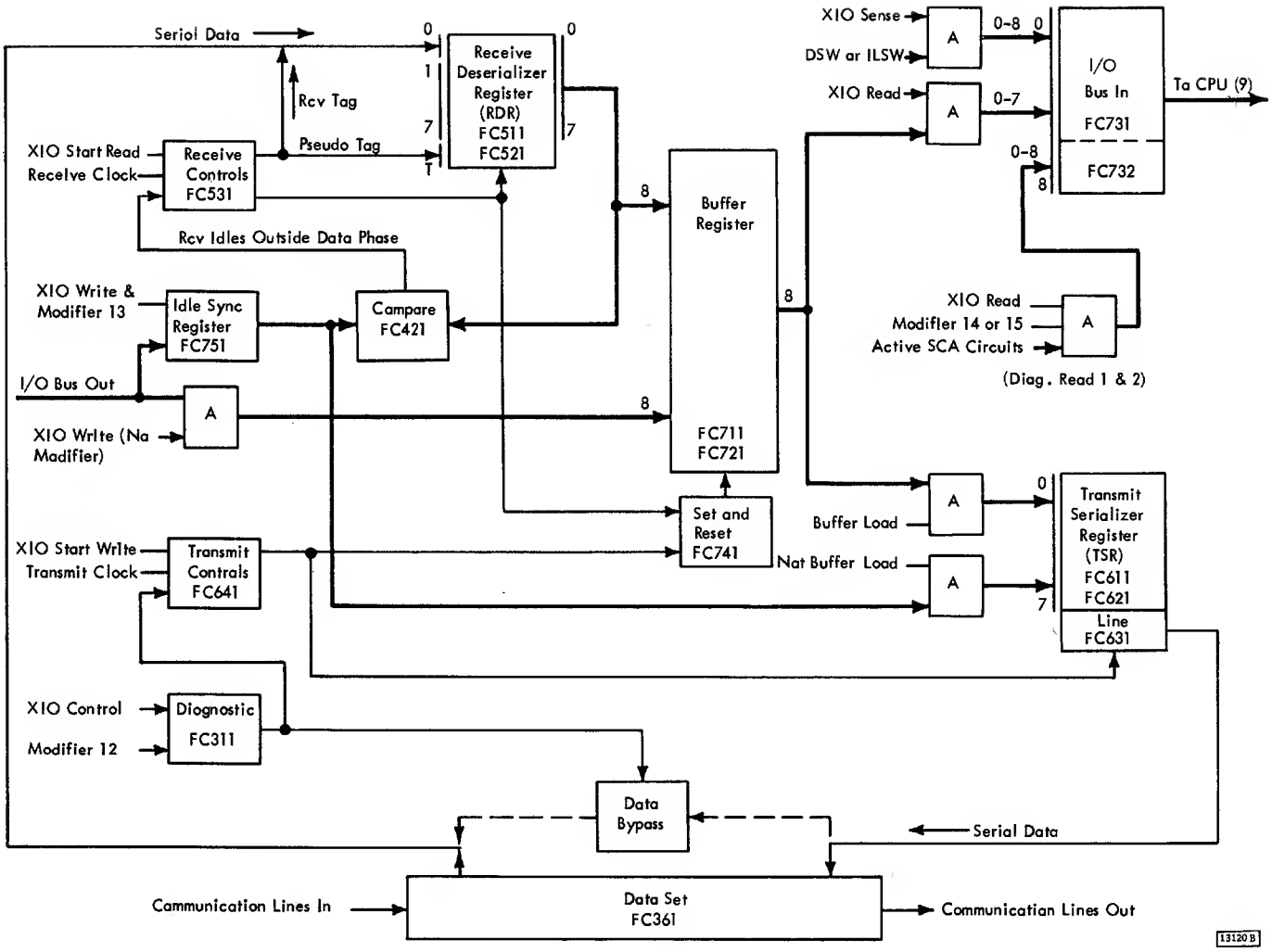


Figure 6-7. Data Flow (SCA)

STR Mode

With usual STR programming, the 'synchronize' instruction turning on the transmit' FL results in turning on the 'clock gate' FL, starting the clocks. Once started, the clocks continue to run until the program gives no more 'transmit' or 'receive' instructions and the 'clock gate' FL is turned off.

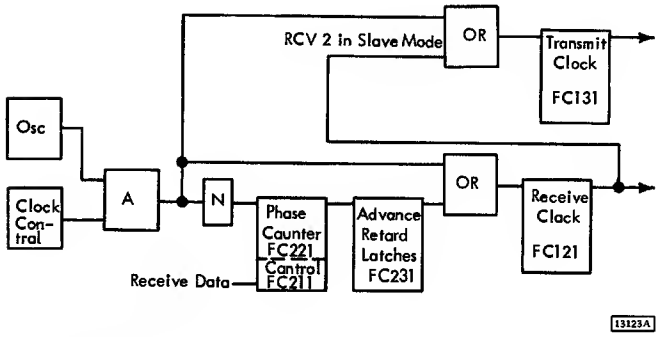


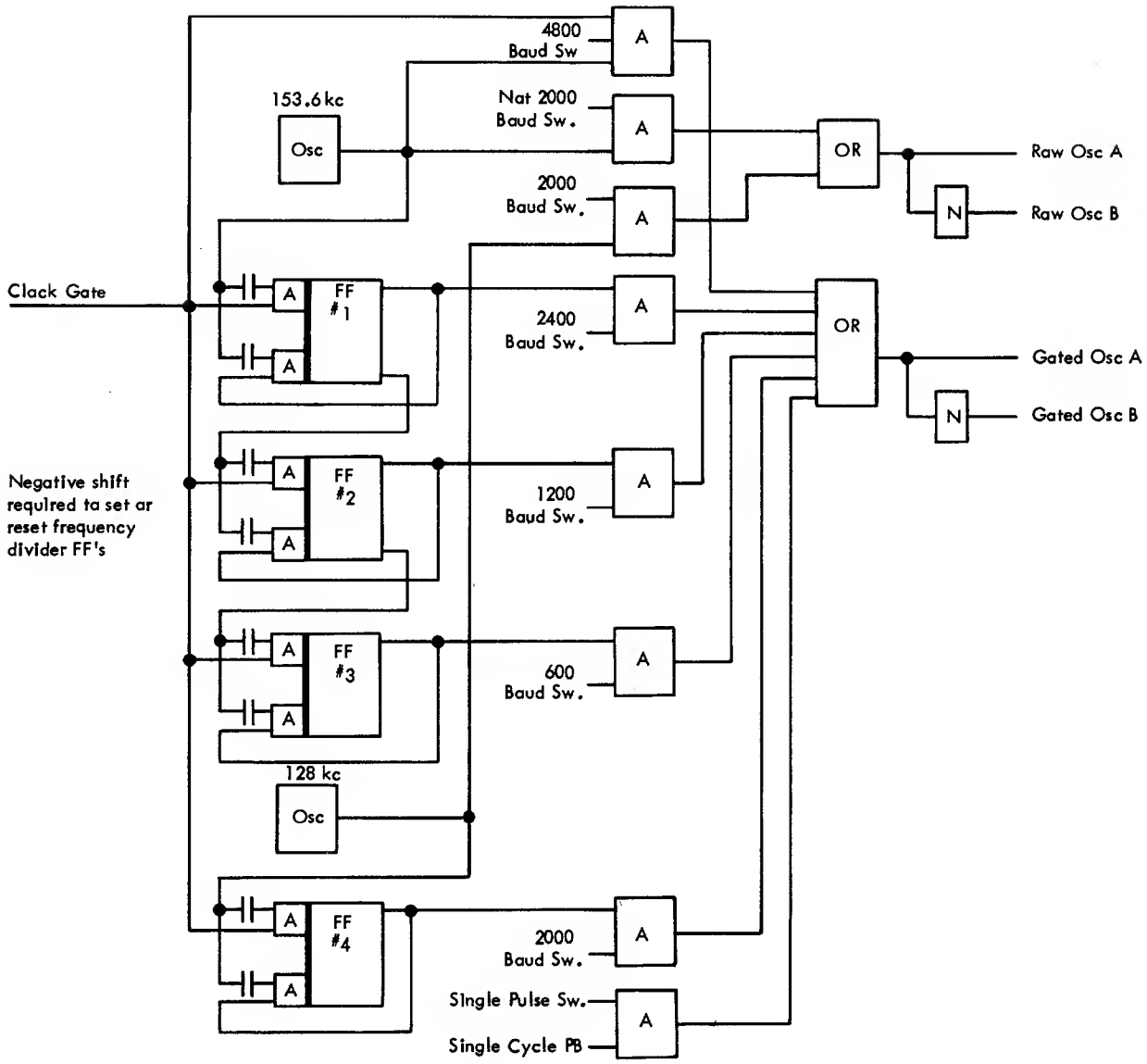
Figure 6-8. Clocks

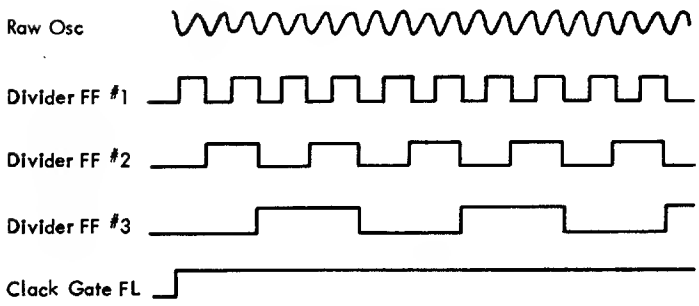
BSC Mode

With usual BSC programming, the clocks may also be started in the same manner if the first instruction is 'synchronize' or 'start write'. However, each time receive mode is entered, the 'clock gate' FL is turned off, and the clocks are stopped. A receive mark to receive space transition turns on 'clock gate' at this time. Should the incoming receive space be "noise", the 'clock gate' FL is reset off, and the clocks stop again. When the incoming receive space level is of sufficient duration, the 'clock gate' FL is left on. The clocks continue to run until receive mode is entered again or the program gives no more 'transmit' or 'receive' instructions.

Diagnostic Mode

Placing the SCA in diagnostic mode also turns on the 'clock gate' FL and starts the clocks. The clocks continue to run until the SCA is removed from diagnostic mode by an 'end op' instruction or a reset.





32 gated asc A and 32 gated asc B per bit time are provided.
Baud = bits/sec.

Bits Per Sec	Clock Pulse	Bit Time	Charocter Time		
			6 Bit*	7 Bit*	8 Bit
600	52 µsec	1.66 ms	9.96 ms	10.62 ms	13.33 ms
1200	26 µsec	.83 ms	4.98 ms	5.81 ms	6.66 ms
2000	15.6 µsec	.50 ms	3.00 ms	3.50 ms	4.00 ms
2400	13 µsec	.415 ms	2.49 ms	2.91 ms	3.33 ms
4800*	6.5 µsec	.208 ms	1.25 ms	1.46 ms	1.66 ms

* BSC mode only

BR0286

Figure 6-9. Clock Drive

Receive Clock

The receive clock consists of the 'R1' and 'R16' flip latches and the 'R2', 'R4', and 'R8' flip-flops. Unless specially controlled by the advance/retard circuits, the clock operates as a binary counter. That is, turning any one position on does not affect the next, but turning any position off changes the

state of the next. The 'R1' FL is turned on by one gated oscillator A pulse and turned off by the next. When the clock is stopped all flip-flops and flip latches are off. The receive clock must be kept in synchronism with the data being received. This is accomplished by the phase counter and advance/retard circuits.

Transmit Clock

The transmit clock consists of five flip-flops -- 'XM1,' 'XM2,' 'XM4,' 'XM8,' and 'XM16.' It operates as a binary counter, with gated oscillator A pulses turning on and turning off the 'XM1' flip-flop. When it is not running all flip-flops are off.

A program instruction can "lock" the transmit clock to the receive clock or allow them to drift with respect to each other. The clocks can be locked together only when the SCA is the "slave" terminal. That is, the 'send receive run' FF is off (in a receive run state). At this time, if the 'character phase memory' FF is on, and the operation is in BSC mode with data terminal clocking or two-wire STR mode, the clocks are locked. Note that turning off the 'R2' flip-flop turns on both 'R4' and 'XM4' flip-flops (FC131). In four-wire STR, regardless of the 'send receive run' FF, the clocks may drift apart. Turning on or turning off the 'send receive run' FF is accomplished by a 'start read,' area 10, with modifier bits 15 or 14, respectively.

Data Terminal and Data Set Clocking

Either of two types of data clocking may be used by the SCA. Data terminal (D/T) clocking, sometimes called internal clocking, uses the transmit clock and receive clock within the adapter circuits to time all shifting of data to or from the communications facility. Data set (D/S) clocking, also referred to as external clocking, uses timing pulses from the data set to time the shifting of data and to control the transmit and receive clocks. Jumpers are installed to select the type of clocking to be used (AD003).

When the jumpers are set for data terminal (D/T) clocking, each transition from 'XM16' to '(not) XM16' (XMO time) in the transmit clock causes a 'transmit shift' pulse. The setting of 'R16' by the receive clock activates the 'receive shift set' pulse (FC361). Each 'transmit shift' pulse shifts the data from the transmit serializer register (TSR) one bit position and resets the transmit clock to 'XMO' time. The 'receive shift set' pulse turns on the 'receive shift' FF, which resets the receive clock to 'R16' time and shifts the incoming data into the receive deserializer register (RDR). Clock adjustments are controlled by the phase counter and advance/retard circuits when using D/T clocking.

When the jumpers are set for data set (D/S) clocking, two lines are furnished by the data set to generate the 'transmit shift' and the 'receive shift set' pulses:

1. 'External transmit timing' generates the 'transmit shift' pulse.
2. 'Receive timing' generates the 'receive shift set' pulse.

These lines, having control of the transmit and receive clock operation, override the attempts of the advance/retard circuitry to adjust the clocks.

> Note: Off-line diagnostic programs may require additional jumpers or jumper changes. Refer to the SCA jumper listing (AD003) and to the description of the diagnostic programs before starting off-line tests.

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PHASE COUNTER AND ADVANCE/RETARD

- Advance/retard circuits attempt to keep the receive strobe pulse centered in the receive data bit times.
- Phase counter aids in determining whether clock advance or retard is required at the end correction cycle time.
- 'Advance/retard (A/R)' latches allow clock advance or retard only after the need is indicated in three consecutive correction cycles.
- 'Memory' FF controls the stepping of the 'A/R' latches according to the value in the phase counter.

The data is received at a bit rate controlled by the remote terminal, while the receive clock rate is determined by the adapter oscillator. It is desirable to have the receive shift sample pulse, sometimes called the receive strobe, near the center of the received bit pulses. The phase counter and advance/retard circuits control the receive clock to maintain, as nearly as practical, this synchronization. To advance the strobe (earlier) the 'R1' flip-latch is turned on an extra time with an oscillator B pulse. To retard the strobe (later) the 'R1' flip-latch is turned off with an oscillator B pulse and at the same time the turn-on of 'R2' is inhibited.

> Note: The timing chart (Figure 6-10) shows that, even when the data timing and receive clock timing are very nearly the same, the receive clock is being repeatedly adjusted by advance and retard pulses.

The time required to transmit the acknowledgment of a received record is relatively short. Thus the SCA reenters receive mode and resumes receive clock adjustment before synchronization is lost.

Phase Counter

The phase counter consists of five flip-flops, designated 'PC [phase counter] 1,' 'PC 2,' ... 'PC 16,' binarily connected, and is able to contain a count of 0 through 31. It is advanced by oscillator B pulses from the start of a data space till the next receive shift and from the end of a data space until the next receive shift. The drive pulses are controlled by the state of the 'receive space' lines and the state of the 'phase counter control' FF (PC ctrl FF).

> Note: Data transmissions are necessary to allow the phase counter operation to maintain bit synchronization. In BSC mode of operation, the terminal may be receiving long messages of continuous 0's or 1's (no data transitions). This could result in the loss of bit synchronization. For this reason, the program in the transmitting terminal must ensure that characters known to have transitions (synchronous idle) are transmitted every 1.25 seconds. The program in the receiving terminal must recognize that these characters are not data but are only for synchronization purposes.

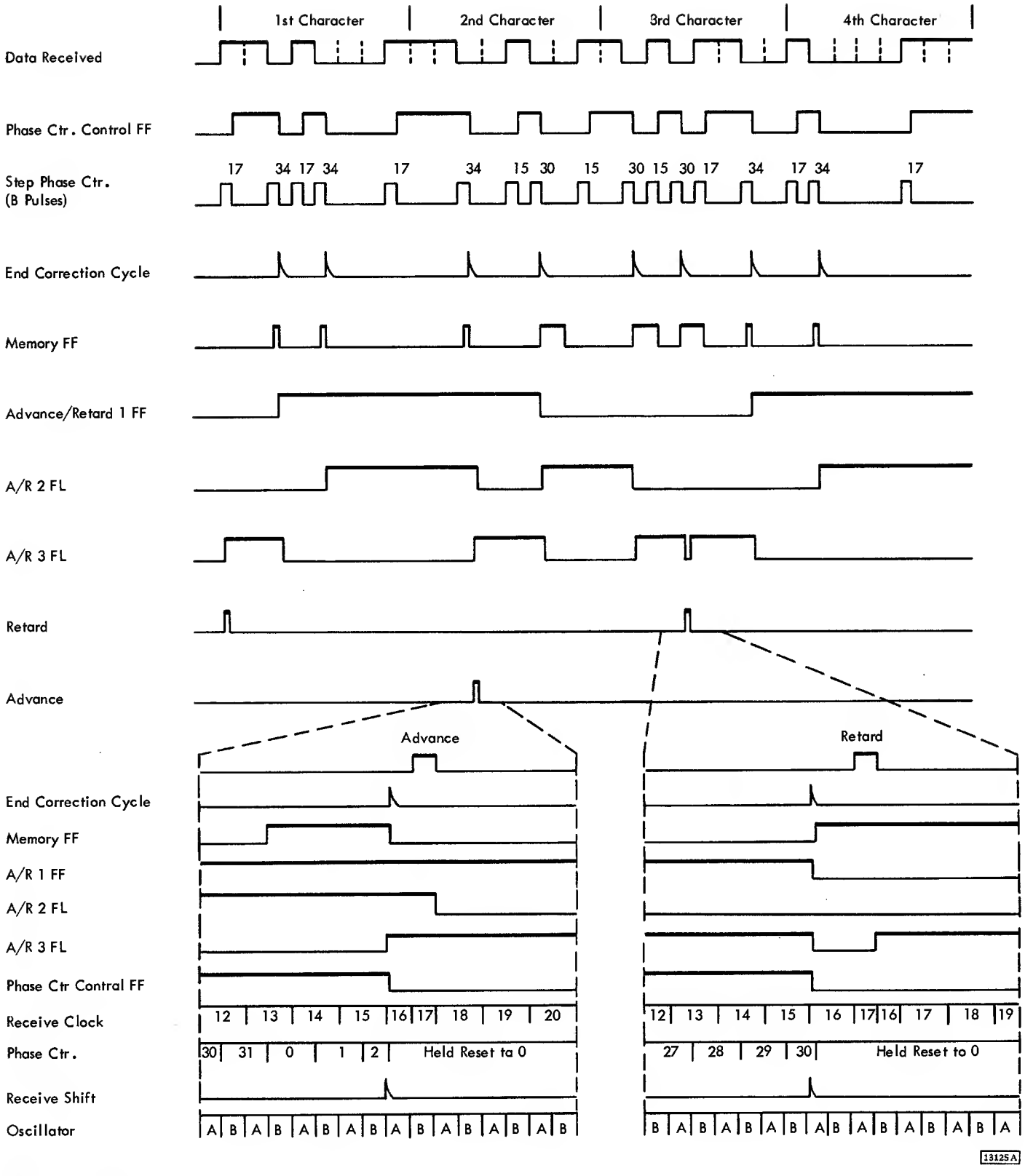


Figure 6-10. Phase Counter

PC Ctrl FF: This flip-flop is turned on by a receive shift sample pulse when a receive space is arriving from the data set. It remains on until a not receive space (receive mark) gate and a receive shift sample pulse turn the flip-flop off.

Step Phase Counter Pulses: These pulses are the output of either of two AND's. One is used at the time of the first mark to space transition of a receive operation if the clocks are stopped. (Remember that only in BSC mode is the clock stopped by entering receive mode.) The second AND is used for all following transitions. Both AND's provide gated oscillator B-pulses to step the phase counter from any transition until the next receive shift sample pulse.

Advance/Retard

Because the frequency of the signals from the data set may vary slightly, no attempt is made to adjust the receive clock at every end correction cycle time (Figure 6-10). Only when a need for adjustment (advance or retard) is indicated for three consecutive correction cycles is the adjustment made. End correction cycle time is the first receive shift following a data space to data mark transition.

The 'advance/retard (A/R)' flip latches and flip-flop provide the means of checking the accumulated need for clock adjustment. When 'A/R1,' 'A/R2,' and 'A/R3' are all on, an oscillator B pulse provides an advance pulse which turns on the 'R1' flip-latch an extra time. When 'A/R1,' 'A/R 2,' and 'A/R 3' are all off, the 'inhibit R2' line becomes active. When 'R1' is on with the 'inhibit R2' line active, the retard line is activated and the following oscillator B-pulse can turn off 'R1' flip latch. This turnoff is prevented from affecting 'R2,' and the result is that the RCV clock is retarded one clock time. Receive clock adjustment occurs only when the SCA is in receive mode if the system is two-wire. If the system is four-wire, the receive clock adjustment is continuous. Remember that, in STR mode, idle characters are being received on one pair of lines while data is being transmitted on the other pair of lines.

The fact that advance or retard action has occurred must be indicated to the 'A/R' latches. At the end of the 'advance' pulse the 'A/R 2' FL is turned off so another advance cannot occur immediately. When the 'retard' line is active, it allows the next oscillator B-pulse to turn on the 'A/R 3' flip latch so that another retard cannot occur at the next end correction cycle time.

Memory Flip-Flop

The 'memory' FF (Figure 6-10) indicates to the 'A/R' latches whether or not the phase counter has reached a count of more or less than 32 at 'end correction cycle' time. A count of 32 or greater means the receive shift, or strobe, is late in the data pulse. In this case the 'PC 16' flip-flop is turned off before the 'end correction cycle' sample pulse. Turning off 'PC 16' turns on the 'memory' FF, which remains on until the next receive strobe. If this is 'end correction cycle' time also, the 'memory' FF being on causes the 'A/R 1' flip-flop to turn on.

A count of less than 32 in the phase counter at 'end correction cycle' time means 'PC 16' has not turned off and the 'memory' FF is not on. At this time 'A/R 1' receives a pulse to turn off, if it is on. Immediately following this time 'reset phase counter' is activated and turns off all PC flip-flops. Any turn-off of 'PC 16' turns on the 'memory' FF. However, the 'memory' FF is turned off by the next receive strobe without affecting the 'A/R 1' flip-flop. 'A/R 1' can only turn on or off at 'end correction cycle' time.

TURNAROUND

- Turnaround occurs when the communicating terminals switch from transmit to receive and vice versa.
- In a four-wire system, turnaround delay is minimal.
- In a two-wire system, turnaround delay includes the 200-ms data set delay.

In a four-wire system, the SCA can be sending and receiving at the same time. However, because the adapter has only a single buffer, the program makes no attempt to send and receive data messages at the same time. Instead, whatever character is stored in the idle-sync register is automatically transmitted over one pair of lines while data is received on the other pair of lines, and vice versa. Thus, the 200-ms turnaround delay is not required to allow line echo to die.

In a half-duplex (two-wire) system, transmission is not possible in both directions at the same time. The SCA can only transmit or receive, and a delay is required for turnaround. This delay consists of any delay required to change modes within the SCA circuits and any delay in the data set. The latter occurs when the 'transmit' FL is turned on and the 'request to send' line is activated. The data set then activates 'clear to send' approximately 200 ms later. On every turnaround one or the other of the terminals requires this delay.

Receive Mode to Transmit Mode

This turnaround is initiated by an 'XIO start write' function and area 10 (turnaround delay occurs in a half-duplex system). Turning on the 'transmit' FL turns off the 'receive' FL, which is self-gated. One of the on-side outputs of the 'transmit' FL activates one input to a singleshot AND (Figure 6-11). The same 'transmit mode' line enters a delay integrator which controls the other input to the singleshot AND. When the 'transmit mode' line becomes active, the output of the AND is immediately active and remains so until the output of the delay line blocks the AND. When the 'transmit mode start SS' line is active (approximately 45 μs), it activates the all turnaround lines (FC331). These lines:

1. Turn off the 'timer' FF.
2. Turn off the 'character phase' FL.
3. Turn off the 'sync counter' FF.
4. Fire the time-out SS.
5. Function in the same manner as the 'reset DSW' line does when active.

Transmit Mode to Receive Mode

This turnaround requires a delay in SCA circuits to ensure that the last character is completely transmitted before turning off the 'transmit' FL. A 'start read' instruction turns on the 'receive' FL, and both 'transmit' and 'receive' flip-latches are on briefly. Then, after the buffer has been emptied of the last character, the 'transmit' FL is reset:

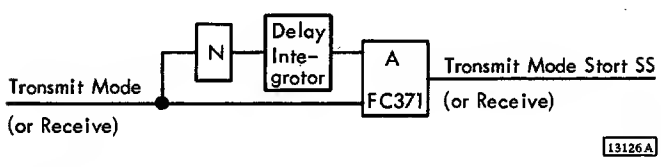


Figure 6-11. Start Singleshots

with the 'receive or end op' line active, the 'buffer empty' signal is ANDed with 'set write response' and 'character phase', causing a character gap check. The next 'transmit shift' then resets the transmit FL, allowing the 'receive mode' lines to be activated. (This same circuitry is used when an end op instruction follows transmit mode to ensure complete last character transmission.) The 'receive mode 2' line fires the receive mode start SS which activates the 'all turnaround' lines previously described, and in BSC mode turns off the 'clock gate' FL. The 200-ms delay then follows as the remote terminal is waiting for its 'clear to send' signal in order to start transmitting (two-wire system). In a four-wire system, this delay occurs only the first time request to send is activated.

REGISTERS

- The registers in the adapter circuits are the buffer, the receive deserializer, the transmit serializer, and the idle-sync.

Buffer Register

The buffer register contains eight flip-flops, which provide intermediate storage for eight bits of data between CPU core storage and the receive deserializer or transmit serializer register. All positions of the buffer register are set or reset at the same time. They are set from the I/O output bus for a transmit operation or from the receive deserializer register for a receive operation. When setting the buffer register, the flip-flops are left off to represent a 1 and turned on to represent a 0. Bus bit 0 through 7 positions gate 'buffer 0' through '7' flip-flops, respectively. When the buffer is reset, all flip-flops are turned off, representing all 1's.

When the buffer register is set with a character the 'buffer load' FL is turned on, and when the character is read out the 'buffer load' FL is turned off. The readout does not reset the register.

Receive Deserializer Register (RDR)

The RDR contains nine flip-flops, which provide temporary storage between the data set and the buffer register for an eight-bit character and a tag bit (Figure 6-12). The flip-flops are turned on to represent a 1 and left off for a 0. All bits received serially from the data set enter RDR bit 0 position, with a receive mark gating the turn-on and a receive space gating the turn-off. The receive shift sample

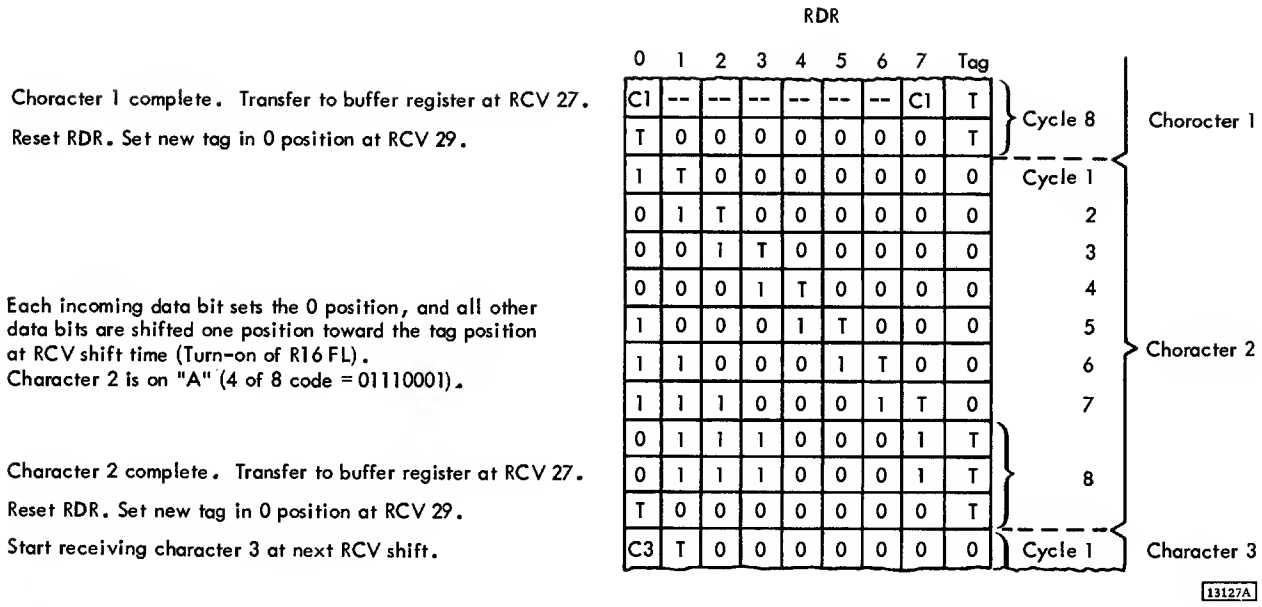


Figure 6-12. Receive Deserializer Register

pulse causes the actual turn-on or turn-off of the flip-flops. Througout the register, the on state of any flip-flop gates the turn-on of the next, and the off state gates the turn-off of the next. Each receive shift sample pulse shifts the on or off conditions of all flip-flops of the register one position toward the tag bit position.

Each time a complete character is present in positions 0 through 7, a tag bit is present in the tag bit position. At this time RDR 0 through 7 positions are transferred to the buffer register in parallel. Then the RDR is cleared and a tag bit set in position 0 by the 'reset deserializer set 0' line. Eight shifts later the tag bit shifts into the RDR 'tag bit' FF, and the next deserializer to buffer transfer occurs.

When the '7 bit frame' FL is on, RDR bit 7 position acts as the tag bit position, and when the '6 bit frame' FL is on, RDR bit 6 position serves as the tag bit position. Thus, fewer clock cycles and a shorter time are required for each character received.

Transmit Serializer Register (TSR)

The TSR contains nine flip-flops, which provide temporary storage between the buffer register and the data set for an eight-bit character and a line bit (Figure 6-13). The flip-flops are turned on to represent a 0 and left off to represent a 1. All positions except the line bit are set in parallel from either the buffer register or the idle-sync register.

TSR bit 0 is set to a 1 on the transmit shift following the character complete condition and at all other shifts is set to a 0. Shifting through the TSR register is effected in the same manner as in the RDR. The state of the 'line bit' FF determines whether the 'transmit data mark bit' line or the 'transmit data space bit' line is activated.

When the 1 which was originally set in TSR bit 0 position shifts into TSR7 position, the last bit of the character is in the line bit position, and bit positions 0 through 6 contain 0's. The 'character complete' FF is turned on, another character is transferred from the buffer register, and the next transmit shift starts the transmission of that character.

When a 7 bit frame code is used, 'character complete' is turned on when the 1 shifts into TSR position 6, and positions 0 through 5 contain 0's. Likewise, when a six-bit frame code is used, 'character complete'is turned on when the 1 shifts into TSR position 5, and positions 0 through 4 contain 0's.

Idle-Sync Register

The idle-sync register contains eight flip-flops, which provide storage for the idle-sync character. It is loaded by an 'XIO write' function, area 10, and a modifier bit 13. The bits of the idle character

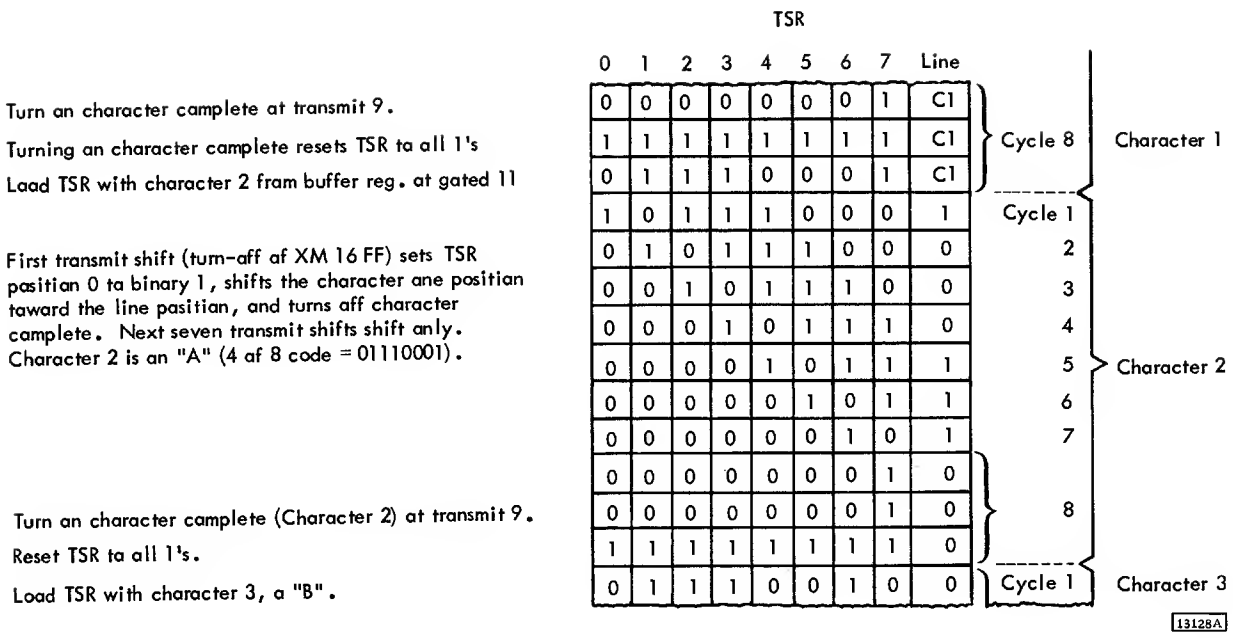


Figure 6-13. Transmit Serializer Register

are read from CPU storage and placed on the I/O output bus. Each bit gates the turn-on of its respective idle-sync register flip-flop. The register is only reset just prior to loading during execution of the instruction.

In transmit operations, the character in the idle-sync register is transferred to the TSR any time the TSR needs another character and the buffer does not have one ready ('buffer load' FL not on). During receive operations, the character in the idle-sync register is continually compared with the character in the RDR. The results of comparison are not used after transfer of data to CPU core storage starts.

CHECK CIRCUITS

- Adapter circuits check only for overrun and character gap.
- Overrun occurs when an attempt is made to set a new character into the buffer register before the previous character has been used.
- Character gap occurs when a new character is needed before one is set into the buffer register.

All checking other than for overrun or character gap (Figure 6-14) is done in the CPU by circuits or program instructions. Adapter circuits (FC741) check for overrun or character gap, either of which results in a check bit 2 in the DSW. Although no interrupt is caused by the check, the bit position should be examined by the program when each read or write response interrupt is serviced.

Overrun

An overrun can occur during either transmit or receive operations. During transmit operations, if the CPU program attempts to reload the buffer register before the character in it has been transferred to the TSR, overrun occurs. The 'write set buffer check overrun' line ANDS with the 'buffer load' FL on to turn on the 'check' FF.

During receive operations, if the adapter circuits attempt to reload the buffer register from RDR before the CPU program has transferred the pre-

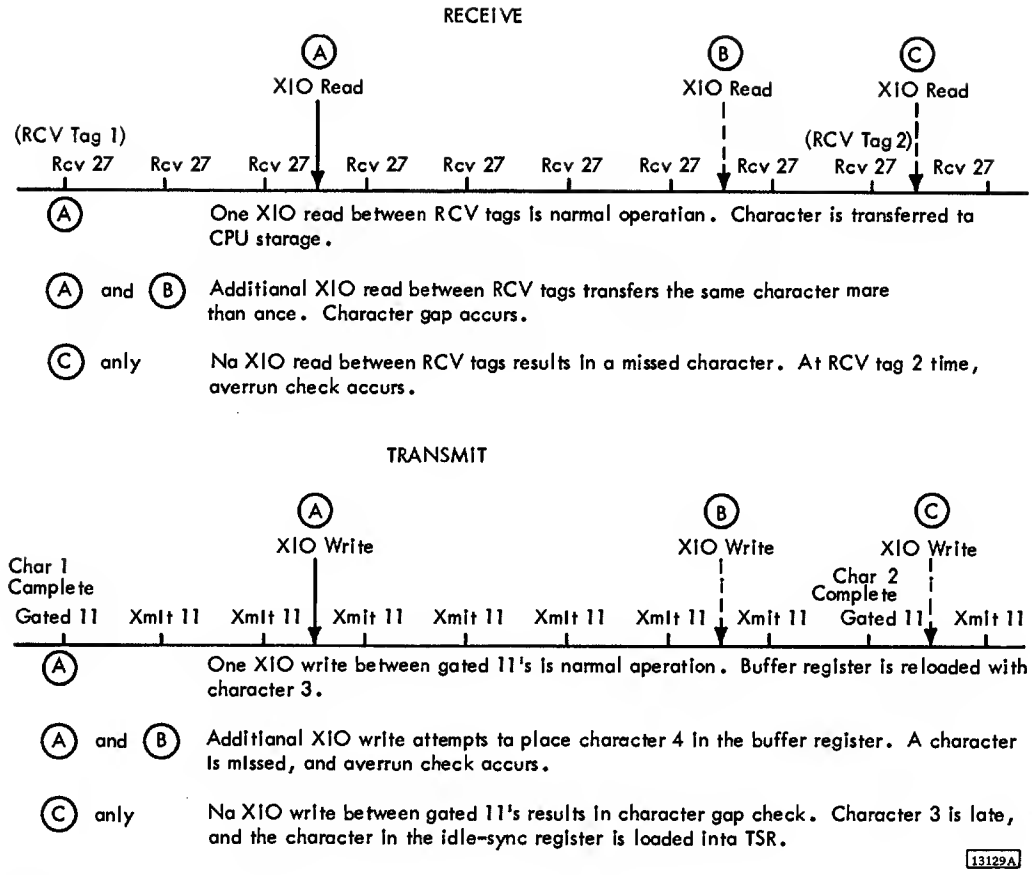


Figure 6-14. Check Conditions (SCA)

vious character from the buffer register to CPU core storage, overrun occurs. Old data remains in the buffer register, and the new data is lost. In this case, the 'set buffer load' line ANDs with the 'buffer load' FL on to turn on the 'check' FF.

Character Gap

A character gap can occur during either transmit or receive operations. During transmit operations, when the character in the buffer register is transferred to the TSR, the 'buffer load' FL is turned off. If the CPU program does not reload the buffer register and turn the 'buffer load' FL on again by the time transmission of the previous character is complete, character gap occurs. The 'set write' response' line ANDs with the 'buffer load' FL off and character phase to turn on the 'check' FF.

During receive operations, when the CPU program transfers a character from the buffer register to the B-register of the CPU, the buffer register is considered to be unloaded, and the 'buffer load' FL is turned off. If the CPU program calls for another transfer from the buffer register to the B-register of the CPU before the buffer register is reloaded from RDR, character gap occurs. The 'read check

gap' line ANDs with 'buffer load' FL off and character phase to turn on the 'check' FF.

FIRST TRANSITION CIRCUITS

- Receive clock is started by the first transition from mark-to-space level of the receive data line.
- Circuits ensure that the clock is not allowed to continue running when started erroneously by line noise.

In the BSC mode of operation, the clocks are stopped when a receive operation starts. The first mark-to-space transition turns on the 'first transition' FF, (FC121). 'First transition', 'receive mode', and 'oscillator A' set the 'clock gate' FL. The 'clock gate' FL may be turned on and the clocks started as a result of line noise which appears to be a 'receive space' signal. Therefore, a check is made of the length of time the receive space level remains after the transition. If the duration is too short there has been a false start, and 'clock gate' and the receive clock are reset off. The adapter then waits for another mark to space transition to again turn on the 'clock gate' FL and start the clock.

With the 'first transition' FF on, the phase counter is stepped by oscillator B pulses as long as the receive space condition exists. If the receive space duration is sufficient, the first receive shift sample pulse turns off the 'first transition' FF, and the operation has a successful start. After the 'clock gate' FL is on, the 'first transition' FF cannot be turned on again.

If the receive space duration is short and ends while the 'first transition' FF is still on, no more step phase counter pulses are generated. The phase counter stops when the receive space condition ends. However, the receive clock continues to run and a receive strobe occurs at 'receive 16' time. As long as the phase counter has a count less than 8, the 'not PC 8 and not 16' line is active. This line ANDs with first transition, receive mode 1, and receive shift trigger to activate the 'reset clock 16 and RCV circuits' line, which turns off the 'clock gate' FL and resets off all receive clock and transmit clock latches. The same line resets all receive deserializer register flip-flops off and turns off the 'character phase' FL and 'CP memory' FF. A "false start" like this occurs for each transition from mark to space not followed by a data space level of at least one-fourth the duration required for data pulses. Once a correct start is made, the circuit is inoperative.

SYNC COUNTER FF

- Flip-flop ensures transmission of at least two synchronization characters at the start in BSC mode.

The 'sync counter' FF ensures that at least two idle-sync characters are transmitted each time transmit mode is entered while the SCA is operating in BSC mode (FC641). The FF is off as transmit is entered because any 'all turnaround' signal turns it off. The shift at the end of the first 'gated 11' turns on the 'sync counter' FF. No write response is set at this time, and the idle-sync character is transferred to the TSR, because the 'buffer load' FL is off (FC741). The second 'gated 11' again transfers the idle-sync character to TSR but sets the 'write response' FF. From then on, the program provides characters for transmission.

PRINCIPLES OF OPERATION

All SLT circuits of the synchronous communications adapter feature are contained on one large board mounted on the C gate of the IBM 1131 Central Processing Unit. Connections to other CPU circuits are made by standard intergate connectors. The interface to the communications data set is shown on the automated logic diagram (ALD) pages FC001 and FC361.

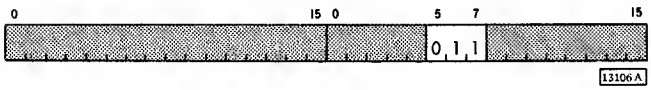
All operations of the feature are started by the CPU encountering an execute I/O (XIO) instruction operation code 00001. The required number of instruction cycles, indexing cycles, and indirect addressing cycles are taken to develop the effective address (EA) of the instruction. The EA must be even, and at EA and EA + 1 is the two-word IOCC.

At the start of execute cycles (E-cycles) the EA is present in the CPU accumulator. Maintenance Diagram AA621 illustrates the CPU operation during E-cycles which is common to all I/O devices. When the control word of the IOCC is present in the temporary accumulator (U register), it is decoded. If the area code (bits 0 through 4) is 01010 (decimal 10), the communications adapter terminal starts to perform the operation specified by the function code (bits 5 through 7) and any modifier bits 8 through 15.

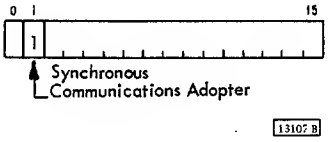
SENSE INTERRUPT (011)

- Sense interrupt sets the ILSW for level 1 in the CPU accumulator when level 1 is the highest active level.

Because the communications adapter causes interrupts on level 1, and because other devices may also interrupt on level 1, the interrupt servicing subroutine must use 'XIO sense' to place the interrupt level status word (ILSW) in the accumulator. The I/O control command (IOCC) is:



If the interrupt was caused by the SCA, execution of this instruction sets the following ILSW for level 1 interrupt in the accumulator:



Decoding the function in the U register activates the 'XIO sense ILSW' line. If at this time the 'interrupt level 1 powered' line and the 'level 1 interrupt request' line are both active, the 'ILSW bit 1' line is activated. This, in turn, develops an I/O bit 1 which is gated to the B-register and later in the CPU cycle transferred to the accumulator.

The 'level 1 interrupt request' line (FC351) is active when any one of these SCA flip-flops is on:

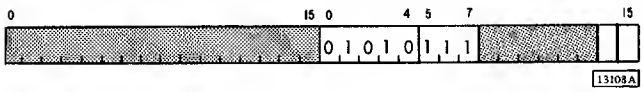
1. Read response.
2. Write response.
3. Time-out.
4. Answer request, while the 'enabled' FF is on.

SENSE DEVICE (111)

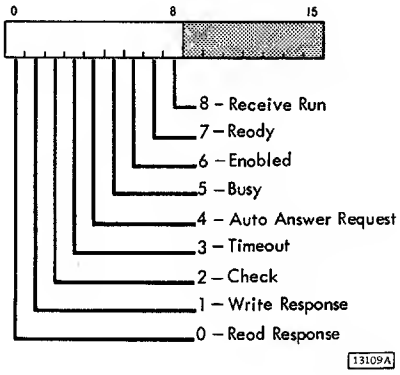
- Sense device sets the DSW for the SCA into the CPU accumulator.

- DSW indicates status conditions within the SCA.

When it has been determined that the SCA caused the interrupt, it is also necessary to give an instruction to sense the condition within the adapter which caused the interrupt. An 'XIO sense' with the following IOCC places the device status word (DSW) in the 1130 accumulator:



The DSW for the SCA follows:



The decoding of the U register activates both the 'XIO sense device' line and the 'area 10' line. These lines gate a group of AND's which activate DSW bit lines (FC731) if their respective indicators are on. The resulting DSW in the CPU accumulator indicates conditions within the adapter circuits.

Significance of DSW Bits

Read Response (Bit 1): A 1 in this position indicates that the 'read response' FF is on. An interrupt is requested because a character has been received and is ready to be transferred to CPU core storage from the SCA buffer register.

Write Response (Bit 1): A 1 in this position indicates that the 'write response' FF is on. An interrupt is requested because another character should be transferred from CPU core storage to the SCA buffer register for transmission.

Check (Bit 2): A 1 in this position indicates that the 'check' FF is on as a result of either an overrun or a character gap.

The overrun condition occurs when the character being transmitted or received attempts to enter the buffer register before the previous character has been read out. Usually the condition is a result of a slow program or a programming error.

The character gap condition occurs when no character is in the buffer register and a transfer is called for. During a transmit operation, the condition occurs because of a slow program. During a receive operation, the condition occurs when a request is made for a character too soon, usually the result of a program error.

In order to prevent an overrun on receive, a character must be transferred to CPU storage from the SCA buffer, following a read response interrupt, within the period shown in Figure 6-15. Also to prevent a character gap on transmission, a character must be transferred from CPU storage to the SCA buffer, following a write response within the period shown in Figure 6-15. The same figure shows the number of characters per second (cps) for each baud. For the SCA, baud is equal to the number of bits per second.

Time-out (Bit 3): A 1 in this position indicates the 'time-out' FF is on, requesting an interrupt. In STR mode, any of three time-outs can activate the interrupt request. They are:

1. Data set time-out. This occurs 3 seconds after the adapter has been instructed to transmit or synchronize, if no 'clear to send' signal is returned by the data set.
2. Transmit time-out. This occurs 1.25 seconds after the adapter has been instructed to synchronize. Write response interrupts are then allowed until the transmit timer latch is turned off. In STR the transmit timer latch turns off when execution of a 'read', 'write' or 'end op' starts. In BSC, the reset occurs as soon as the interrupt is requested.
3. Receive time-out. This occurs every 3 seconds while the SCA is in receive mode. The same timer is used as is used for a data set time-out.

In BSC mode of operation, an additional program timer is available. This timer can be started by a control instruction with a 1 in modifier position 10 of the IOCC control word. The time-out interrupt request occurs 0.35 seconds later. Turning on the program timer resets the transmit and receive timers.

All timers can be turned off by a singleshot fired by any of three conditions.

1. An 'XIO sense device' instruction with a 1 in modifier bit position 14.
2. An 'all turnaround' signal.
3. The circuit which activates the time-out interrupt request.

Auto Answer Request (Bit 4): A 1 in this position indicates that the 'answer request' FF is on as a result of receiving a ring indicator signal from the data set. Note that only if the 'enabled' FF is on does 'answer request' cause a level 1 interrupt request.

Busy (Bit 5): A 1 in this position indicates that either the 'receive' FL or the 'transmit' FL is on. Turning off both the 'receive' FL and the 'transmit' FL makes the SCA "not busy."

Enabled (Bit 6): A 1 in this position indicates that the 'enabled' FF is on. A 'control' instruction with a modifier bit 8 turns on the 'enabled' FF, and it stays on until another 'control' instruction with a modifier bit 9 turns it off. While the 'enabled' FF is on, the adapter can activate an interrupt request as a result of a 'ring indicator' signal from the data set.

Time Between Characters

Baud \ Char. Size	6 Bit	7 Bit	8 Bit
600	10.0 ms	11.6 ms	13.3 ms
1200	5.0 ms	5.8 ms	6.6 ms
2000	3.0 ms	3.5 ms	4.0 ms
2400	2.5 ms	2.9 ms	3.3 ms

Character Rate

Baud \ Char. Size	6 Bit	7 Bit	8 Bit
600	100 cps	85.7 cps	75 cps
1200	200 cps	171 cps	150 cps
2000	333.3 cps	286 cps	250 cps
2400	400 cps	343 cps	300 cps

30024 B

Figure 6-15. Timings

Ready (Bit 7): A 1 in this position indicates that the data set is connected and ready to transmit or receive. A dial-up data set must have received a data terminal ready signal from the adapter.

Receive Run (Bit 8): A 1 in this position indicates that the 'send receive run' FF is off. When this FF is off, the adapter is in a receive run condition, operating as the "slave" terminal. This is the normal reset condition and a program instruction is required to establish the SCA as the "master" terminal. Turning the 'send receive run' FF on sets the adapter to a send run condition, making it the "master" terminal. Except when the system is four wire and operating in STR mode or when using D/S clocking, the 'receive run' condition locks the transmit clock to the receive clock, whenever the 'CP memory' FF is on.

The 'send receive run' FF is turned on by a 'start read' instruction with a modifier bit 15 and turned off by a similar instruction with a modifier bit 14.

Sense Reset

When the 'XIO sense device' IOCC control word contains a 1 in bit 15 position, execution of the sense DSW instruction turns off the condition in the adapter which caused the interrupt.

When the IOCC control word contains a 1 in bit 14 position, the timer reset is activated. This resets off any timer that is running.

A bit 15 in the control word of the IOCC activates the 'XIO sense reset 15' line at T6 of an E2 cycle. This line in the adapter circuits ANDs with 'XIO sense device' and 'area 10' to activate the 'DSW reset' line (FC371). This line ORs with 'all turn around' to turn off any of these flip-flops for which the corresponding DSW bit is active:

1. Read response.
2. Write response.
3 Time-out.
4. Answer request.

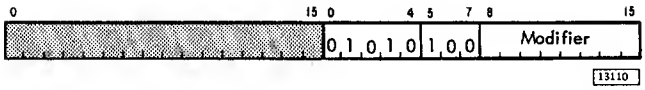
The 'check' FF is reset off by this line at any time it is on.

The turn-off for the other indicators has been included in the descriptions of the indicators.

CONTROL (100)

- Control function code sets up the adapter circuits to perform operations further defined by the modifier bits in the IOCC.

The 'XIO control' instruction affects the operation of the communications adapter in a manner determined by the modifier bits of the IOCC. The IOCC is:



Decoding of the control function code activates the 'XIO control' line, which ANDs with an 'area 10' line and a 'T6' pulse. This conditions a sample pulse driver and causes a sample pulse (negative shift) on the 'gated control' line (FC311). The functions which are initiated at this time are dependent on which modifier bits are present in the IOCC control word.

Enable SCA (Bit 8): A 1 in this position places the adapter in a status such that it can interrupt on receipt of a "ring indicator" signal from the data set.

The 'gated control' pulse turns on the 'enabled' FF (FC341) when a bit 8 is present in the U-register. The 'enabled' FF being on allows a level 1 interrupt request to occur when the 'answer request' FF is turned on by a ring indicator signal from the data set.

The 'enabled' FF also gates the DSW bit 6 and turns on a console indicator.

Disable SCA (Bit 9): A 1 in this position removes the adapter from the enabled status.

Bit 9 in the U-register gates the turn-off of the 'enabled' FF, and 'gated control' turns it off. The flip-flop has no function when it is off.

Start/Stop Time-out (Bit 10): A 1 in this position changes the state of the 'timer' flip-flop (FF). Turning this flip-flop on resets the receive timer and the transmit timer. In BSC mode, turning on the 'timer' FF starts the program timer.

Bit 10 in the U-register gates both the turn-on and the turn-off of the 'timer' FF (FC341). Execution of the instruction when the 'timer' FF is off turns the FF on, and vice versa. Turning on the 'timer' FF in BSC mode starts the program timer, which causes a time-out interrupt request after 0.35 seconds. When the timer FF is on, it resets and prevents activating either the receive timer or the transmit timer and their resulting time-out interrupts.

Either a second identical instruction, executed while the 'timer' FF is on, or the time-out interrupt turns off the 'timer' FF. It can also be turned off by 'all turn around,' 'end op,' or 'dc reset.'

Synchronize (Bit 11): A 1 in this position of the IOCC starts the synchronization procedure. It turns on the 'transmit' flip-latch (FL) and causes sending of idle or sync characters. In STR, idles are transmitted for 1.25 seconds before a write response is allowed. In BSC, only two sync characters are transmitted before the first write response.

If the SCA is not already in transmit mode when this instruction is given, a turnaround occurs. The turnaround, with a 1 in position 0, 1, 3, or 4 of the address word in the IOCC resets the corresponding position of the DSW (i.e., read response, write response, time-out, or auto answer request).

Bit 11 in the U-register allows the 'gated control' pulse to turn on the 'synchronize trigger' FF (FC321) and to activate the 'start write diagnostic or sync' line (FC311).

Turning the 'synchronize trigger' FF on does these things:

1. Turns off the 'end op' trigger, if it is on.
2. Blocks the allow write response line.
3. Turns on the 'transmit' FL and starts the transmit timer, which turns on the 'transmit timer latch' 1.25 seconds later. This instruction causes idle characters to be transmitted for 1.25 second during STR mode. Only two idle-sync characters are sent automatically in BSC mode. (Also see "Start Write.")

The 'synchronize trigger' FF is turned off by activating the 'start read write or end op' line with a later instruction.

Thc 'start write diagnostic or sync' line (FC311) fires the end op reset SS (FC331) and turns off the 'buffer load' FL.

Diagnostic (Bit 12): A 1 in this position establishes a continuous wraparound mode of operation with the adapter circuits electronically disconnected from the data set until the next SCA 'end op' instruction or a dc reset.

Data flow in the diagnostic mode is from the buffer register to the transmit serializer register to the receive deserializer register and back to the buffer register. In this mode, a read response interrupt request occurs at each bit shift time, and a special diagnostic subroutine is used for maintenance procedures.

Bit 12 in the U-register allows the 'gated control' pulse to turn on the 'diagnostic' FF, placing the adapter in diagnostic mode (FC311). The flip-flop can be turned off by either the 'end op' FF turning on or activating the 'dc reset' line.

Modifier bit 12 also activates the 'start write diagnostic or sync' line, firing the end op reset SS (FC331) and turning off the 'buffer load' FL.

End Op (Bit 13): A 1 in this position causes the turning off of major controls which were turned on for transmit, receive, or diagnostic operations. A transmit operation is not ended until a character gap is sensed and an automatic circuit delay is complete. This procedure ensures that the last character reaches the communications line before the transmit mode is turned off.

Bit 13 in the U-register allows the 'gated control' pulse to turn on the 'end op trigger' FF (FC321). Turning the flip-flop on:

1. Turns off the 'receive' FL.
2. Turns off the 'diagnostic' FF.
3. Activates the 'start read write or end op' line (FC311), which ensures that the 'synchronize trigger' FF turns off.
4. Fires the 1.0-ms delay SS if the SCA is just leaving receive mode (FC741). This maintains the data terminal ready condition until the SS times out.
5. Activates the 'receive or end op' line (FC311), which prevents any write responses (FC351).
6. Activates the 'reset or all turnaround or end op' line (FC341), which turns off the 'timer' FF and resets the phase counter.

The functions which are actually performed by the 'end op' depend on the previous mode -- synchronize, transmit, receive, or diagnostic.

Six-bit Frame (Bit 14): A 1 in this position sets the adapter circuits to operate with a frame or character length of six bits.

Seven-bit Frame (Bit 15): A 1 in this position sets the adapter circuits to operate with a frame length of seven bits.

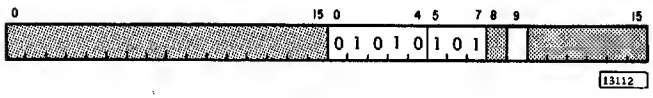
> Note: Frame length can be changed at any time to six bits or seven bits by a control instruction with the proper modifier bit. However, once the frame length is set at six or seven, either an 'end op' instruction or a dc reset is required

to return to the eight-bit frame length. Only BSC mode allows the use of six-bit or seven-bit frames.

START WRITE (101)

- Start write initiates a transmit operation.
- DC reset to SCA circuits can be programmed.
- Resulting turnaround can be used to reset certain bits in the DSW.

The start write function code sets the SCA to transmit mode and calls on the data set for transmit service. The IOCC is:



A modifier bit 9 in the IOCC causes a programmed dc reset of SCA circuits. This results in a short duration impulse which accomplishes the same functions in the adapter circuits as pressing the CPU reset pushbutton.

If the SCA is not already in transmit mode when this instruction is given, a turnaround occurs. The turnaround, with a 1 in position 0, 1, 3, or 4 of the address word in the IOCC, resets the corresponding position of the DSW (i.e. read response, write response, time-out, or auto answer request).

The start write function code activates the 'XIO start write' pulse to adapter circuits and this ANDs with an 'area 10' line to activate the 'start read write end op' line. The same pulse also turns on the 'transmit' FL. This activates the transmit mode lines and blocks the receive mode lines, turning off the 'receive' FL if it was on. Once turned on, the 'transmit' FL stays on until after the next turn-on of either the 'receive FL or the 'end op' FF. At that time, 'set write response' and 'buffer empty' are ANDed with 'character phase' causing a character gap check, which sets the 'check' FF. 'Check' is then ANDed with the next 'transmit shift' to reset the 'transmit' FL. This ensures that the last data character has been processed by the SCA.

Turning on the 'transmit' FL places the SCA in transmit mode. The 'transmit mode' lines:

1. Turn off the 'receive' FL and block receive mode (FC311).
2. Turn on the 'clock gate' FL if the SCA is not in CE mode (FC111).
3. Activate the 'data terminal ready' line to the data set and activate 'busy' (FC331). In a full-duplex (four-wire) system, these lines are always active.
4. Activate the 'request to send' line to the data set (FC361), if the system is two-wire (jumper installed), and the SCA is not in diagnostic mode. In a four-wire system, the jumper is not in place, and transmit mode is not necessary to activate 'request to send.'
5. Fire the transmit mode start SS, which activates the 'all turn around' lines.
6. Start the 3-second receive timer while waiting for the 'clear to send' from the data set.

All Turn Around

The 'all turn around' lines perform several functions when they are activated. These are:

1. Turn off the 'timer' FF (FC341), and reset the phase counter (FC211).
2. Turn off the 'character phase' FL (FC531).
3. Turn off the 'sync counter' FF (FC641).
4. Reset any interrupt request flip-flop if its corresponding bit is in the CPU B-register. This reset can be assured by entering 'FF00' in the address word of the IOCC of a 'synchronize' or 'start write' instruction which causes the 'all turn around' lines to be activated.
5. Reset the 'check' FF.
6. Fire the time-out SS. This resets any timer which may be on.

Clear to Send

The 'clear to send' line is activated by the data set about 200 ms after the 'request to send' is activated to the data set. In a half-duplex (two-wire) system 'request to send' is not activated until transmit mode is entered (FC361). In a full-duplex (four-wire) system 'request to send' is active all the time. Once 'clear to send' is activated it remains active as long as 'request to send' remains active. Four-wire STR mode allows the SCA to transmit idle character continuously at the same time it is receiving data.

Transmit Start

STR

No data characters are transmitted until the clear to send line is activated by the data set. Then in STR two-wire operation, one complete idle character is automatically transmitted before any data characters. Assuming the idle-sync register has previously been set with the idle character (see "Write -- Modifier Bit 13"), the procedure is as follows:

1. At transmit 9 time, when the transmit serializer register flip-flops 0 through 6 are on, indicating binary 0's in those positions, the 'character complete' FF is turned on. Turning on 'character complete' resets the TSR to all 1's.
2. At the following transmit 11 time (gated 11), a sample pulse is generated which transfers the idle-sync register to the TSR, because the 'buffer load' FL is off. A gated 11 occurs at transmit 11 time only if 'character complete' is on (FC641). In STR mode, 'set write response' is activated at this time.
3. Each transmit 0 time (not XM16), a transmit shift sample pulse shifts all bits in the TSR toward the low-order position, bit 0 to bit 1..., bit 7 to line bit.
4. At the first shift time for any character, as the first bit is shifted into the 'line bit' position, a 1 is set in bit 0 position of the TSR to act as a "transmit tag." At succeeding shift times, a 0 is set in this position.
5. The status of the 'line bit' FF determines whether a data mark or a data space is sent to the data set.
6. When the transmit tag 1 shifts into the TSR bit 7 position at the eighth transmit shift time, the last character bit is shifted to the 'line bit' position and is available to the data set. Remember that 6 bit or 7 bit frame length cause TSR positions 6 or 7 to function as the 'line bit' position does from 8 bit frame length.

Turning on the 'write response' FF (step 2) activates the 'level 1 interrupt request' lines (FC 351). While the idle character is being transmitted, the CPU program must service the interrupt request by transferring a data character from core storage to the buffer register. When this is done, the 'buffer load' FL is turned on so that at the next interrupt the TSR can be loaded from the buffer register.

At the time of the first write response, the 'character phase' FL (FC531) is not on. Therefore, a character gap is not indicated by activating the 'check' line as a result of the 'buffer load' FL being off (FC741). The 'character phase' FL is turned on by the shift at the end of the first write response. Checks can then be set during the remainder of the transmit operation.

BSC

In BSC mode, it is required that at least two idle-sync characters precede the first data character. The first 'gated 11' cannot set write response because the 'sync counter' FF is off (FC641). At the end of 'gated 11' time, the 'sync counter' FF turns on. The first write response then occurs at the second 'gated 11', by which time one idle-sync character has been transmitted. The character in the idle-sync register is transferred to the TSR for a second time, and is transmitted. The CPU program must provide all following characters for transmission.

When the 'transmit' FL is turned on as a result of a 'synchronize' instruction in STR mode, the 'synchronize trigger' FF on blocks the 'allow write response' line (FC341). After 1.25 seconds, the 'transmit timer latch' turns on, and the first write response interrupt request occurs. During the time that no write responses are allowed, at each 'gated 11,' the idle-sync register contents are transferred to the TSR and transmitted. At the time of the first write response, one more idle character is set in the TSR and transmitted. The CPU program services the interrupt and provides the following characters for transmission. These might be EOI sequence, INQ sequence, etc.

When the 'transmit' FL is turned on as a result of a 'synchronize' instruction in BSC mode, only two characters from the idle-sync registers are transmitted automatically. The 'sync counter' FF controls the 'set write response' line just as it does for a 'start write' instruction.

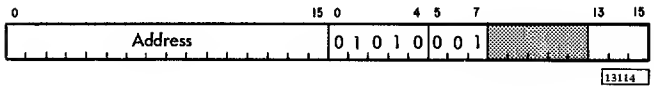
WRITE (001)

- XIO instruction with a write function code in the IOCC is given in the level 1 interrupt servicing subroutine.

- Write function transfers data to the SCA adapter.

- Data can enter the buffer register or the idle-sync register, depending on a modifier bit in the IOCC control word.
- Write function can start or stop the audible alarm.
- Maintenance Diagrams 65-20, 65-30, 65-40.

The 'write' instruction is used in the interrupt level 1 servicing subroutine. Execution of the instruction causes transfer of a character from CPU core storage to the adapter buffer register, from which it is later transferred to the transmit serializer register for transmission. The IOCC is:



The address word contains the CPU core storage address from which the character is placed in the buffer for a transmit operation. As each character is transmitted, the program must modify the address word to obtain succeeding characters of the message. When the IOCC control word (2nd word) contains a bit 13, the character in B0 through B7 of the CPU B-register is transferred to the idle-sync register of the communications adapter. In any case, the character transferred is the high-order half of the word specified by the address portion of the IOCC.

When the IOCC control word of an 'XIO write' instruction contains a bit 14, the alarm is turned on, and conversely a bit 15 turns off the alarm. The alarm is usually programmed to turn on when:

1. Character synchronization is lost.
2. The TEL sequence is received.
3. The EOT sequence is received.
4. A program-determined number of unsuccessful attempts are made to transmit a record.

Note: Operating the alarm and loading the idle-sync register can be done by one instruction, if desired.

No Modifier Bits

The 'write' instruction transfers a character from CPU storage to the SCA buffer register. From there it is later transferred to the TSR and transmitted. The write function, decoded from the U-register, causes the CPU to enter a third execute cycle (E3). At T4 time of this cycle, if the IOCC contains no modifier bits 13, 14, or 15 and the buffer is empty ('buffer load' FL off), the 'write mode buffer reset' line is activated (FC311). All flip-flops in the buffer register are turned off, clearing the last previous character from the register and setting all positions to 1s.

At T6 time of the same E3 cycle, the 'write set buffer check overrun' line is activated for the duration of T6. This line (FC741) checks the status of the 'buffer load' FL, and if it is off, activates the 'transfer B-register to buffer' line. The end of the T6 pulse generates a 'buffer set' sample pulse and turns on the 'buffer load' FL. For each position of the B-register which contains a 1, the corresponding FF in the SCA buffer register is left turned off. If there is a 0 from the CPU, the corresponding FF is turned on. (B0 through B7 are transferred to the buffer register 0 through 7 positions, respectively.)

The character in the buffer register remains there until the next time the 'character complete' FF is turned on signifying that the TSR is empty. At this time, a 'gated 11' pulse activates the 'set write response' line. This line checks the 'buffer load' FL. If it is on, as it should be, the start of the 'gated 11' activates the 'transfer buffer to transmit serializer' sample pulse. The character set in the buffer register by the 'write' instruction is transferred to the TSR. Also at 'gated 11' time, the 'write response' FF is again turned on and another 'level 1 interrupt request' signal generated. This signal indicates to the CPU that the character in the buffer register has been read and transferred to the TSR. The end of the 'set write response' turns off 'buffer load'. The CPU program should now reload the buffer register by another 'write' instruction.

Note: At 'gated 11' time, the TSR is loaded from the buffer register if the 'buffer load' FL is on. If it is off, the TSR is loaded from the idle-sync register, and a 'character gap' check is indicated.

Modifier Bit 13

This bit present in the IOCC of a 'write' instruction (FC311) causes the data transferred on the E3 cycle to be set in the idle-sync register instead of in the buffer register. At T4 time, the idle-sync register is reset (all flip-flops turned off). At T6 time, those

'B bit' lines (FC751) which are active (logical 1's) allow the corresponding idle-sync register flip-flops to turn on.

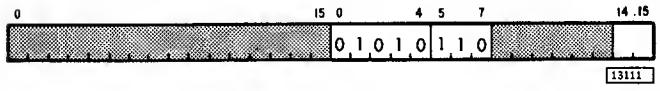
Modifier Bits 14 and 15

These modifier bits in the IOCC for a 'write' instruction control the alarm. At T6 of an E3 cycle, if bit 14 position of the U-register contains a 1, the 'alarm' FF is turned on (FC321). A similar instruction with a modifier bit 15 turns off the 'alarm' FF. The flip-flop can also be turned off by a dc reset. The alarm can be stopped by setting the alarm console switch off. However, the alarm restarts when the switch is set back on, unless the 'alarm' FF is turned off.

START READ (110)

- 'Start read' initiates a receive operation.
- Resulting turnaround can be used to reset the DSW.
- Receiving of data starts when character phase is established.
- An interrupt occurs for each data character received.
- Modifier bits 14 and 15 determine the "master" or "slave" status of the SCA.
- Maintenance Diagrams: 65-60, 65-80, 65-100, 65-110

The 'start read' instruction sets the communications adapter to a receive condition and calls on the data set for receive service. The IOCC is:



Modifier bit 15 establishes the SCA as the "master" terminal in order to send messages. Modifier bit 14 makes the SCA a "slave" terminal in order to receive messages in STR mode. In BSC mode, the SCA is usually left as the "slave" terminal, which is the reset condition.

Receive Mode Start

The 'start read' instruction in the CPU program prepares the SCA circuits to receive serial data from the communications data set. Decoding the U-register during the E2 cycle activates the 'XIO start read' line and the 'area 10' line. ANDing these lines gives a voltage shift which turns on the 'receive' FL (FC311) and activates the 'start read area 10' line and the 'start read write or end op' line. The shift as 'start read area 10' is activated can turn on or turn off the 'send receive run' FF (FC211) if there is a 1 in the U-register position 15 or 14 respectively. The shift as 'start read write or end op' is activated turns off the 'synchronize trigger' FF (FC321), if it was on.

The 'receive mode' lines can only be activated immediately if the 'transmit' FL is off. If the 'transmit' FL is on when the 'receive' FL is turned on, both remain on long enough to ensure that the last bit has shifted out of the TSR line-bit position. This delay is accomplished by ANDing 'receive or end op', 'check' (character gap), and 'transmit shift'. The 'transmit' FL is then reset. Character gap check does not occur until 'set write response' is active with 'buffer empty' and 'character phase' (FC741). The next 'transmit shift' then allows a reset to the 'transmit' FL, and the 'receive mode' line becomes active.

The 'receive mode' line becoming active fires the 'receive mode start' SS, activating the 'all turn around' lines. In addition BSC mode and the receive mode start singleshot turn off the 'clock gate' FL (FC111). Thus, the clocks are stopped when receive mode is entered in BSC.

As described previously in "STR Special Programming," the program can set the idle-sync register so that the SCA can recognize a CL or TL character. This is necessary for communication with devices which do not always transmit at least one idle character preceding control or data characters.

Receive Mode

After receive mode is entered, character phase must be established in order to enter data phase and receive data (see 65-110, FEMDM). The procedure required depends on whether operation is in STR or BSC mode.

Character Phase (STR)

Establishment of character phase in STR mode requires the receipt of one character like that presently in the idle-sync register. When the 'receive' instruction is the one given while attempting to start "handshaking," the 'CP memory' FF is not yet on. If the SCA has been "handshaking," the 'CP memory' FF is on. In either case, the clocks are running from a previous instruction.

Each receive clock cycle, turning on the 'R16' FL fires the receive shift sample pulse driver (SPD). At each 'RCV shift' time the receive data-space line is sampled (FC511). If it is at a RCV mark level (receive data bit is binary 1), the sample pulse turns on the 'RDR bit 0' FF. Conversely, a RCV space level (binary 0) turns off the 'RDR bit 0' FF. The 0's and 1's are shifted through the RDR at each 'RCV shift' time. The idle-sync register must previously have been set with the idle character (see "Write" -- "Modifier Bit 13"). The outputs of the RDR flip-flops and the idle-sync register flip-flops are constantly entering the idle-sync compare circuits (FC421).

As the RDR is receiving and shifting bits from the data set, at some 'RCV shift' time, RDR contains a complete idle character, and the 'idle-sync' line from the compare circuit becomes active. The following RCV 27 time turns on the 'idle character' FL (FC531), which activates the 'set pseudo tag' line, if the 'CP memory' FF is off (FC531). This line turns on the 'RDR tag bit' FF, activating the 'RCV tag' lines. As soon as 'RCV tag' is activated, the 'character phase' FL and 'CP memory' FF are turned on.

The operation with the 'CP memory' FF already on is slightly different. In this case, entering receive mode turns on the 'idle character' FL immediately. Framing has been completed, and tag bits are shifting through RDR. Even though receiving may start anywhere in a character, the tag indicates the end of one character and start of another. Therefore at the time RDR contains a complete idle character, the 'RCV tag' lines will also be active, and all conditions are met to turn on 'character phase' (FC531).

When 'character phase' has been turned on, the 'idle character' FL can no longer be turned on. However, it remains on until the first non-idle character is in RDR. Then, at 'RCV 25' of 'RCV tag' time, 'idle character' is turned off, and 'data phase' becomes active for the rest of 'receive tag' time. Thereafter 'data phase' is active throughout each 'RCV tag' time. For the remainder of character phase, the SCA treats all received characters as data characters.

Character Phase (BSC)

Establishment of character phase in BSC requires the receipt of two consecutive characters like that presently in the idle-sync register. The 'receive mode start' SS stops the clocks when receive mode is entered, and they must be restarted. With the 'clock gate' FL off, the first transition from a 'receive mark' to a 'receive space' sets the 'first transition' FF. The 'first transition' FF with 'RCV mode 1', turns on the 'clock gate' FL (FC111) and starts the clocks. The first transition circuits (see Chapter 2) check that the mark to space transition was not merely line noise.

Receiving of bits and comparison of RDR and the idle-sync register proceed as in STR with the 'CP memory' FF off. When the idle-sync compare is equal, the 'idle character' FL turns on at 'RCV 27.' 'Set pseudo tag' is activated and turns on the bit 6, bit 7, and tag bit positions in RDR, activating the 'RCV tag' lines, regardless of the frame length which may be presently set. 'RCV tag,' 'RCV 29,' and 'idle character' activate the 'reset desrl set 0' line. This inserts a "tag" which shifts through RDR ahead of the next character.

Search starts for the second successive character like that in the idle-sync register. Note that in BSC mode 'character phase' cannot be set until 'RCV 25' of the next 'RCV tag' time. At that time, if there is no idle-sync compare equal, the 'idle character' FL is turned off. This means that only one character like that in the idle-sync register has been received, and 'character phase' does not turn on. A new search for two successive idle-sync characters starts.

When the first equal compare occurs, the 'idle character' FL turns on at 'RCV 27' as previously described. If a second successive idle-sync compare equal occurs at the next 'RCV tag' time, 'character phase' and 'CP memory' turn on at 'RCV 25.' Thereafter, the 'idle character' FL cannot be turned on again while 'character phase' remains on. 'Idle character' remains on until the first non-idle character is received. Then 'idle character' turns off, and 'data phase' is activated at each 'RCV tag' time.

CP Memory FF

STR Mode

Once turned on, the 'CP memory' FF (FC371) can only be turned off by a time-out, a dc reset, or by the SCA becoming not busy (not receive and not transmit). The 'character phase' FL turns off at each turnaround, but the 'CP memory' FF stays on.

BSC Mode

The 'CP memory' FF is turned off each time receive mode is entered when the SCA is operating in BSC mode, because the 'reset clock 16 and RCV circuits' line is activated (FC111). Therefore, in BSC mode, at least two idle characters are always required for establishment of character phase.

Receiving Data Characters

Each time the tag bit shifts into the RDR tag bit position, the RCV tag line becomes active, indicating that a complete character is set in RDR. After the required idle characters have been recognized, the presence of a non-idle (data) character in RDR turns off the 'idle character' FL at RCV 25 time. 'Not idle character', 'RCV mode 4', 'character phase' and 'RCV tag' condition the data phase AND so that, at each following 'RCV tag' time, these lines can be activated:

1. At 'RCV 25' time, 'buffer reset' (FC531), if the 'buffer load' FL is off.
2. At 'RCV 27' time, 'transfer deserializer to buffer,' if the 'buffer load' FL is off.
3. At 'RCV' 27 time, 'set buffer load,' to indicate that the buffer register has been loaded.
4. 'Data phase or diagnostic,' during all of 'RCV tag' time.

The first three lines cause the character presently in the RDR to be transferred to the buffer register. The fourth gates the turn-on of the 'read response' FF at the end of 'RCV 27' time. Turning on the 'read response' FF activates the 'level 1 interrupt request' line, signaling the CPU that a character is available to it.

Any idle characters received during 'character phase' do not turn on the 'idle character' FL and are transferred to the CPU as data characters. Any analysis of these characters must be accomplished by the CPU program.

Modifier Bit 15

A 1 in the U-register bit 15 position gates the turn-on of the 'send receive run' FF by a 'start read area 10' signal (FC211). The SCA is established as the "master" unit when this flip-flop is on.

Modifer Bit 14

A 1 in U-register bit 14 position gates the turn-off of the 'send receive run' FF by a 'start read area 10' signal, making the SCA the "slave" unit.

The 'send receive run' FF in the off state activates the 'RCV run' line (FC211). When the 'CP memory' FF is on, the 'RCV run' line locks the transmit clock to the receive clock (FC131) if the system is operating under one of the following conditions:

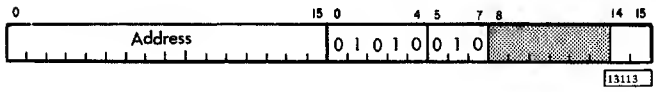
1. D/T clocking and half-duplex (two-wire) with STR or BSC communication.
2. D/T clocking and full-duplex (four-wire) with BSC communication.

The 'R4' FF and the 'XM4' FF both turn on when 'R2' turns off.

READ (010)

- XIO instruction with a read function code in the IOCC is given in the level 1 interrupt servicing subroutine.
- Read function transfers data from the SCA adapter to the CPU.
- Modifier bits 15 and 14 in the IOCC control word cause the transfer of diagnostic read words 1 and 2, respectively.
- Maintenance Diagrams: 65-90, 65-100, 65-110.

The 'read' instruction is used in the interrupt level 1 servicing subroutine. Execution of the instruction causes transfer of a received character from the buffer register to CPU core storage. The IOCC is:



The address word contains the CPU core storage address at which the received character is stored when the instruction is executed. The program must modify the address word as each character is received and stored. Bits 13, 14, and 15 must be 0's to transfer the buffer register.

When the IOCC contains a 1 in position 15 of the control word, diagnostic read word 1 is transferred to CPU core storage at the address specified by the address word of the IOCC. Diagnostic read word 2 is transferred when position 14 of the IOCC contains a 1. Each position of the diagnostic read words is set to 1 when its assigned line or latch in the SCA circuits is activated or turned on.

No Modifier Bits

The 'read' instruction in the CPU program transfers a received character from the SCA buffer register to CPU core storage. The read function, decoded from the U-register, causes the CPU to enter a third execute cycle (E3). From T1 through T6 of this cycle, the 'XIO read' line is active. This line ANDs with 'not bit 13, 14 or 15' (FC731). The output of this AND is exclusive ORed with a service voltage, and the output of the exclusive OR is active when the inputs are different (T1 through T6 of the E3 cycle). The exclusive OR acts as a powering inverter. With this line active and 'area 10' decoded from the U-register, the presence of a 1 in the buffer register activates the corresponding 'SCA data bit' line to the I/O bus in.

The T6 pulse in this cycle activates the 'read-check gap' line, turning off the 'buffer load' FL. If it is already off, an error condition exists (see Chapter 2 -- "Check Circuits").

Modifier Bits 14 and 15

The presence of a modifier bit 15 blocks the 'not bit 13, 14 or 15, line (FC321). This prevents the transfer of the buffer register contents to the I/O bus in. Instead, the 'U bit 15' line ANDs with 'XIO read' to activate the 'diagnostic read 1' line (FC732) and transfer diagnostic read word 1 to the CPU. This line and 'area 10' condition a group of AND's which cause the "on" state of various SCA flip-flops and flip-latches or the active state of control lines to activate the 'diagnostic read 1 bit 0' through '9' lines. These lines set 1's on the I/O bus in to be stored in CPU core storage, as follows:

Bit 0 Synchronize trigger FF
Bit 1 Idle character FL
Bit 2 Character complete FF
Bit 3 End op trigger FF
Bit 4 Diagnostic FF
Bit 5 Timer FF
Bit 6 3-second receive timer
Bit 7 1.25-second transmit timer
Bit 8 Send data space bit line

The presence of a modifier bit 14 activates the 'diagnostic read 2' line and causes a different group of adapter lines to set diagnostic read word 2 on the I/O bus in, as follows:

Bit 0 Clock gate FL
Bit 1 Sync counter FF
Bit 2 First transition FF
Bit 3 Phase counter control FF
Bit 4 Receive tag line
Bit 5 Character phase FL
Bit 6 Available for CE use
Bit 7 Pushbutton latch
Bit 8 Available for CE use

DIAGNOSTIC MODE

- Diagnostic mode is entered by giving an XIO control instruction with bit 12 = 1 in the IOCC control word.
- Bits shifted out of the transmit serializer register enter the receive deserializer register.
- An interrupt occurs each time the bits in RDR are shifted.
- Special diagnostic programming can make effective use of diagnostic mode.
- Maintenance Diagrams: 65-20, FC707.

Turning on the 'diagnostic' FF by activating 'XIO control,' 'area 10,' and 'U bit 12 powered' at T6 time places the SCA in diagnostic mode. It remains in diagnostic mode until it receives an 'end op' instruction or a dc reset. While running in diagnostic mode, bits are shifted from the line position of TSR to the high order or bit 0 position of the RDR. Remember that TSR shifts at 'XM0' time, and RDR shifts at 'RCV 16' time. Each time a bit is shifted in RDR a level 1 interrupt request is activated to the CPU. This interrupt request is a result of turning on the 'read response' FF (FC351) at each 'RCV 27' time when the turn-on is gated by the 'data phase/diagnostic' line being active in diagnostic mode.

Most effective use of the diagnostic mode is possible only with a diagnostic program in the CPU. Usually such a program is entered after an 'end op' instruction or dc reset, so that conditions within SCA circuits are known. The exact format of a diagnostic program is not fixed, but one possible sequence of operations is described here, and a timing chart appears on ALD page FC705.

1. Following the 'end op' instruction, the SCA is placed in diagnostic mode. This establishes a "wrap-around" data path and prevents data from going to the data set.

2. Next a 'write' instruction loads the buffer register with some known data character. From there, the character is transferred to the TSR at the next 'gated 11' time. (The first 'xmit 11' is a 'gated 11' because the 'character complete' FF is turned on as diagnostic mode is entered.) In STR mode, a 'write response' occurs at this same time but can be ignored by the program. In BSC mode, no write response can occur until the second and succeeding 'gated 11's, because the 'sync counter' FF is not turned on until the end of the first 'gated 11.'
3. The first read response occurs after a bit has been shifted from the TSR line position to the RDR bit 0 position. This bit may be either a 1 or a 0, because it is the last or high order bit of some previous character. (A dc reset would have turned off the 'line bit' FF, representing a binary 1.) The program services this and succeeding read response interrupt requests by read instructions which transfer the contents of the buffer register to core storage. After the ninth read response has been serviced, the complete known eight-bit character has been transferred through the TSR, to the RDR, and into core storage. Note that a six-bit or seven-bit frame could be set, and the number of read responses for a complete character would be decreased.
4. By program, a detailed analysis can be made of the operation of the functional units involved in the diagnostic mode. After the analysis is made, the program may give error typeouts, repeat the operation with the same or different character, or proceed with other types of diagnostic programs.

   Note: The time available for program execution between interrupts at the higher bit rates is so short that the diagnostic program should be run alone.

FEATURES

There are no features for the IBM 1130 Computing System Synchronous Communications Adapter.

POWER SUPPLIES AND CONTROLS

One small additional power supply is required when the SCA feature is installed. It supplies -12 Vdc, is rated at 1/4 ampere, and is installed at the bottom of SLT gate C which contains all SCA circuits. The -12 Vdc is supplied to the oscillators and the converter (CV) cards. All other voltages are supplied by the standard power supplies of the 1131.

There are no added power sequencing circuits when the SCA is installed.

CONSOLE AND MAINTENANCE FEATURES

CONSOLE INDICATORS

Additional indicators are installed in the CPU console when the synchronous communications adapter feature is included in the IBM 1130 system. These indicators are described in the order in which they appear on the console, left to right in the lowest row of indicators.

Ready (RDY)

This indicator lights when the data set is ready. The most commonly used data sets do not signal ready (FC361) until they receive the data terminal ready signal from the SCA. However, some data sets give the ready indication as soon as power is turned on.

Enabled (ABL)

This indicator lights when the CPU program turns on the 'enabled' FF (FC341), which allows the SCA to activate an interrupt request on receipt of a ring indicator signal from the data set.

Receive (REC)

This indicator lights when the 'receive' FL (FC311) is turned on. Note that on a turnaround from transmit mode to receive mode, the receive and transmit indicators are on together briefly.

Transmit (TSM)

This indicator lights when the 'transmit' FL is on (FC311).

Buffer Load (BFR)

This indicator lights when the 'buffer load' FL is on (FC741). This indicates that the character presently in the buffer register has not been read out to the B-register or to the TSR.

Clock Running (CLK)

This indicator lights when the 'R2' flip-flop of the receive clock is on (FC141). When the receive clock is running, the 'R2' FF is on approximately one-half the time. Remember that when one clock runs, both clocks should run.

Data In (DI)

This indicator lights when the 'receive data-space' line from the data set is at a receive space level, or when the CE mode switch is on and the CE space switch is set to 'space' (FC411). Note that, in a two-wire system, the indicator may also light during transmit operations. This is a result of the 'echo' from space bits being transmitted.

Character Phase (CP)

This indicator lights when the 'character phase' FL is on (FC531). Remember the importance of establishing character phase in receive operations.

CE INDICATOR CARDS

The use of the CE indicator cards is described on ALD pages FC761 and FC771. These cards can be used to display the contents of the idle/sync register, receive deserializer register (RDR) and the transmit serializer register (TSR). In CE mode, data can be shifted one bit at a time and displayed on the indicator cards to verify correct operation. Note that RDR indicators light when the position does not contain a logical 1, and TSR indicators light when the position does contain a logical 1.

CONSOLE AND CE SWITCHES

All switches except the alarm switch are located on the operator's panel of the CPU. They are described in the order in which they appear, left to right (Figure 6-16).

STR/BSC Switch

This switch selects the mode in which the SCA operates. The correct program must be used.

Set to STR

1. In a two-wire system, ensures that 'gated 11' pulses occur only when the adapter is in transmit mode.

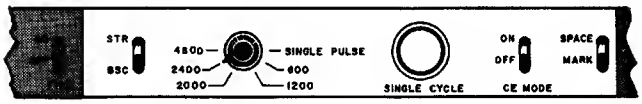


Figure 6-16. Operator Panel

2. Allows 'time-out' to turn off the 'CP memory' FF.
3. When 'CP memory' is off, gates the start of the 'end correction cycle' singleshot.
4. Prevents 'set pseudo tag' from turning on 'bit 6' or 'bit 7' in RDR.
5. Gates the 'set write response' line after the 45-microsecond SS times out.
6. In a four-wire system, gates the 'transfer sync register to transmit serializer' at 'gated 11' while in receive mode.

Set to BSC

1. Allows the 'receive mode start SS' to reset the transmit clock, receive clock, and 'clock gate' FL. At the same time, 'reset clock 16 and receive circuits' line is activated.
2. Gates the locking together of the transmit and receive clocks, when 'receive run' is active and the 'CP memory' FF is on.
3. Gates the use of the program timer.
4. Gates 'clear to send' when the SCA is in transmit mode.
5. Gates the 'reset transmit timer latch' line. The latch can be reset by 'time-out' or 'XIO sense device,' ' area 10', and 'U bit 14' active together.
6. Allows 'set CP memory trigger' line to be activated only at 'receive 25' time, when the other conditions are met ('idle character' FL on, 'receive tag' active, etc.).
7. Allows the on side of the 'sync counter' FF to affect the activating of the 'set write response' line.
8. Allows the use of six-bit and seven-bit frame lengths.

Speed Selection Switch

This rotary switch (FC411) is set to establish the number of bits per second which are transmitted or received. In actual practice, the switch setting determines the frequency of gated oscillator A and gated oscillator B pulses. The switch also

has a single pulse position to allow the CE single cycle pushbutton to provide gated A- and B-pulses.

CE Single Cycle Pushbutton

This pushbutton switch (FC411) controls the 'push-button latch' (PB latch). When the pushbutton is pressed, the latch turns on, and when it is released, the 'PB latch' turns off. Turning on the 'PB latch' while the clocks are running, turns off the 'clock gate' FL at the next transmit shift time (FC111). Turning on the PB latch when the clocks are stopped and the CE mode switch is on causes the clocks to run for one cycle.

When the speed selection switch is set to the single pulse position, pressing the single cycle pushbutton and turning on the 'PB latch' activates and 'gated oscillator A' line. Releasing the push-button activates the 'gated oscillator B' line. In this operation, the pushbutton must be pressed 32 times to step through one clock cycle.

CE Mode Switch

When this switch is turned on, it performs these functions:

1. Blocks control of the 'RCV space' line by the 'RCV data-space' line from the data set, and gates control by the CE space switch (FC411).
2. Blocks the turn-on of the 'clock gate' FL by transmit or diagnostic mode, and allows the CE single cycle pushbutton to turn it on (FC111).
3. Blocks the turn-on of 'character complete' FF at the start of diagnostic mode (FC641).

Turning off the CE mode switch causes a 'dc reset' to the SCA circuits.

The purpose of CE mode is to allow the CE to service the SCA independent of the customer's operation on the remainder of the system. SCA failures can be analyzed by running off-line diagnostics. However, since diagnostics require the use of other areas of the system, they should be run at the customer's convenience with the intent of looking for the failure in CE mode once the failing area is determined.

The CE mode of operation can be altered, as required, to any one of the following modes, or a combination of these modes, by the use of jumpers:

1. Off-line mode
2. Force receive mode
3. Force transmit mode
4. Allow interrupts in diagnostic mode
5. Allow continuous clock run
6. Receive line data in CE mode

Refer to ALD page AD003 and The Field Engineering Maintenance Manual, IBM 1130 Computing System, Order No. SY26-5977, for jumper connections and the procedure for their use.

Normally, in CE mode, all SCA interrupts are inhibited. By installing the appropriate jumper, interrupts are allowed only when the SCA is in diagnostic mode and CE mode -- for example, when running the SCA display program.

With the off-line jumper removed, the SCA is in on-line mode, but remains independent of CPU operation while in CE mode. After loading the idle/sync register with a predetermined bit pattern, this pattern can be continuously transmitted, in on-line mode, to a remote receiving station. Also, idle characters or data (non idle) characters can be continuously received from a remote station to check the character phase and data phase circuitry. If the 'buffer' light on the SCA console is on, data phase has been established.

Off-line mode means that the SCA is operating independently of the CPU and is not connected to the telephone lines. If the jumper is installed for off-line mode, characters being sent from the transmit serializer register (TSR) are switched to the receive deserializer register (RDR) by setting the test/operate switch on the data set cable to the test position. Depending on the setting of the baud rate switch and the use of additional jumpers, data is shifted from the TSR to the RDR in either single clock pulse (32 pulses per bit), bit by bit, or continuously by pressing the pushbutton.

Force receive mode (with the SCA off-line and in CE mode) provides a means of checking the character phase circuitry and the shifting of bits in the RDR. This is accomplished by using the CE space switch to present a bit pattern to the RDR. Each depression of the pushbutton shifts the bits in the RDR one position towards the tag position and shifts one bit into the RDR. Bit 7 arrives first, then 6, 5, 4, etc. If the bit pattern sent matches the bit pattern in the idle/sync register, character phase should be established. Continuous force transmit or force receive operation allows scoping of the transmit or receive circuitry.

CE Space Switch

This switch is effective only when the CE mode switch is on. Then, the CE space switch determines the level of the 'RCV space' line (FC411), forcing a receive space level when on and a receive mark level when off.

Alarm Switch

This switch on the console keyboard is another means of stopping the alarm, should the program not turn off the 'alarm' FF (FC321). However, if the switch is set on again before the 'alarm' FF is turned off, the alarm restarts.

INTRODUCTION

FUNCTIONS OF THE IBM 2501 CARD READER

- Two models of the 2501 (A1 and A2) are available (Figure 7-1).
- Either model provides high-speed card input to the system.
- Reading speed of the model A1 is 600 cards per minute; that of the model A2 is 1000 cards per minute.
- Either model provides the program load function, even though other readers are also included in the system.

The IBM 2501 Card Reader, available in two models (A1 and A2) provides high-speed input from cards to an 1130 system. The 2501 can be connected to any 1131 CPU except models 1A and 1B. However, the 2501 cannot be installed in an 1130 system which includes an IBM 1231 Optical Mark Page Reader.

In a system including both a 2501 card reader and another device that normally can provide the program load function, only the 2501 can perform this function.

The 2501 reads cards (photocells sense the holes) one column at a time, starting in column 1. Once a read operation has started, the entire card passes through the read station without stopping (Figure 7-2). Data is transferred to the CPU during cycle steal (CS) cycles for each column. The number of columns from which the data is transferred can be controlled by the program. After

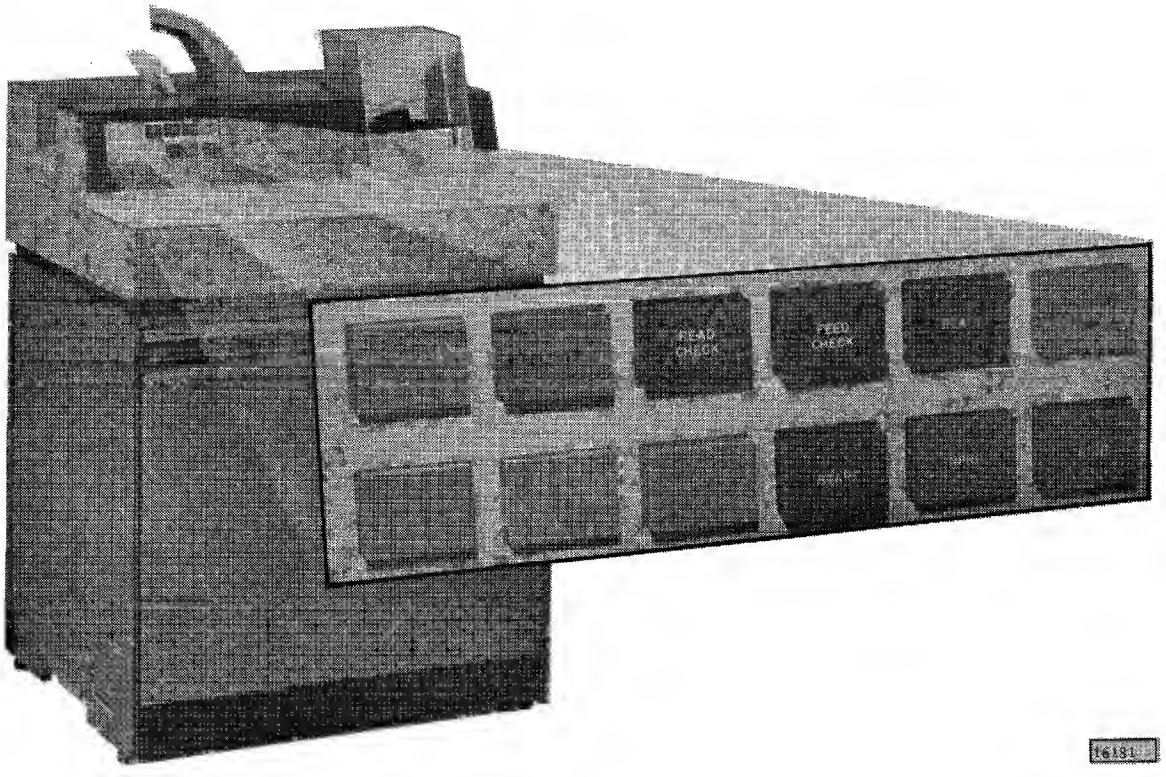


Figure 7-1. IBM 2501 Card Reader

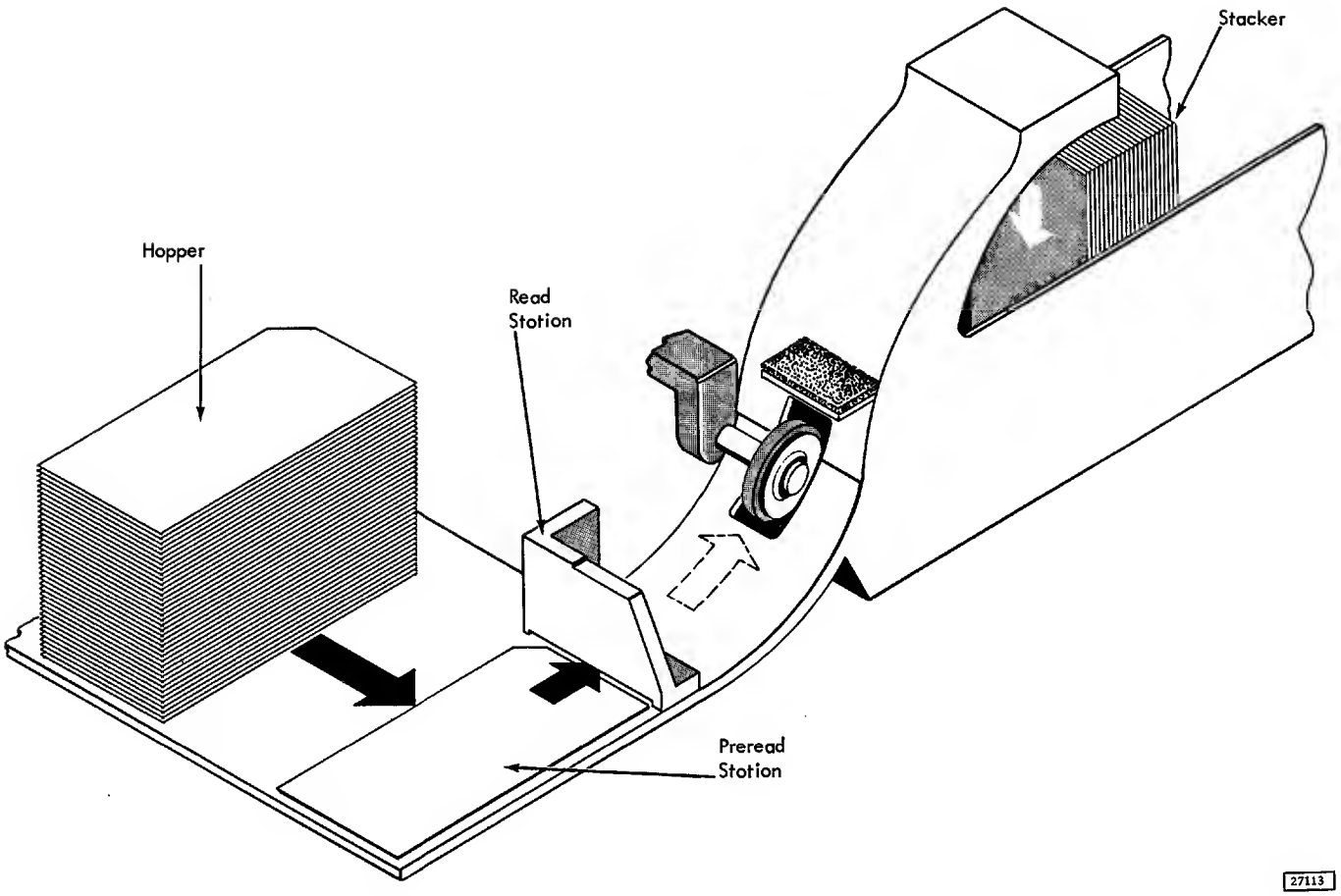


Figure 7-2. 2501 Card Path

each feed cycle, the 2501 activates a level 4 interrupt request to the CPU.

ADAPTER CONNECTIONS

- Control and timing pulse lines to the adapter set the adapter circuits to start an operation of the 2501.
- Area code for the 2501 is decimal 9 (01001).
- Adapter-to-2501 lines activate magnets and indicators in the 2501 and control the circuits of the 2501.
- 2501-to-adapter lines indicate to the adapter the conditions within the 2501 and supply the read data.
- Adapter-to-CPU lines signal when CS cycles and interrupts are requested and provide the data to the CPU.
- Maintenance Diagram FR401.

CPU to Adapter

When the CPU executes an XIO instruction, decoding of the control word of the IOCC activates control lines to all I/O adapters. An area code of 9 (01001) causes these lines to affect the adapter circuits for the 2501. The control lines that are applicable to the 2501 adapter are:

1. XIO sense ILSW.
2. XIO sense device.
3. XIO start read (initiate read).
4. XIO sense reset 15.

The 'program load to 2501' line is activated when the CPU program load key is pressed. The result is a program load operation. No instruction is necessary to start a program load operation.

Control lines are activated to provide CPU timing pulses to the adapter and to indicate to the adapter certain CPU conditions; e.g., 'CPU run' and 'power on reset.' Data lines from the CPU provide for loading the card reader core address register in the adapter. The same data lines are used, on another cycle, to load the word count register in the card reader (CR) adapter.

Adapter to 2501

Control and signal lines from the adapter to the 2501 device cause magnets to be energized, indicators to light, and so on. These lines are shown in FR401, the data flow diagram for the 2501 adapter. Both the start-run controls and the read controls, shown in this diagram, are in the adapter circuits.

2501 to Adapter

Control and signal lines from the 2501 to the adapter provide timing pulses connected with the read operation in the 2501. Emitter and CB pulses are examples of this type of signal. Also, data lines make the read solar cell outputs available for setting the CR register in the adapter.

Adapter to CPU

Control and signal lines from the adapter to the CPU indicate conditions within the adapter to the CPU. Examples are the lines that indicate ready or busy. Also, the adapter activates cycle steal and interrupt requests and provides lines for transferring read data and bits of the DSW and ILSW.

READ OPERATION

- Read operation is started by initiate read function code.
- Run-in to preread station is required to make the 2501 ready before the first initiate read code.
- Holes in each column are sensed by photocells to set the CR register.
- Each column is sensed a second time. A difference in the sensings indicates an error.
- Data transfer to the CPU occurs during CS cycles and stops when the word count is reached.
- After all 80 columns have passed the photocells, a level 4 interrupt request occurs.

Before any XIO instruction with the initiate read function is given, the 2501 must be made ready. A card must be fed into the preread station by pressing the start key.

Card reading is started by a program 'initiate read' command. The card is fed through the reading station during the second card feed cycle (first card read cycle). This causes columns 1 through 80 of the card to be read in one continuous motion of the card. The card is read serially -- that is, column by column -- beginning with column 1. Reading is accomplished by the photocell sensing mechanism (Figure 7-3). While each card column is being sensed by the photocells, the data is set into the adapter read register. Then the photocell output is re-sampled and compared with the output of the buffer register. If the compare is unequal, the error check indicator is set.

Each column of data is read, placed in the register and checked, then transferred to the B-register by cycle steal cycles. Data transfer (Figure 7-4) begins with the data read from column 1 of the card and continues until the word count equals 0. The instruction specifies the address of the word count. The data from column 1 is set into the core storage location following that of the word count. Succeeding data is set into successively higher-numbered locations.

This read, check, and cycle steal process continues until the word count equals 0. Then data transfer stops, although part of the card may not have been read. An end operation response causes a level 4 interrupt request at the end of the feed cycle.

Data Coding

The 2501 reads any combination of punches in any card column. Any code translation required must be done by the stored program. During normal read operations, the twelve rows (12-9) in a card column correspond to the 0-11 bits, respectively, in the core storage word (Figure 7-4).

Last-Card Sequence

When the hopper empties during a feed cycle, the 2501 is taken out of ready status. The operator can

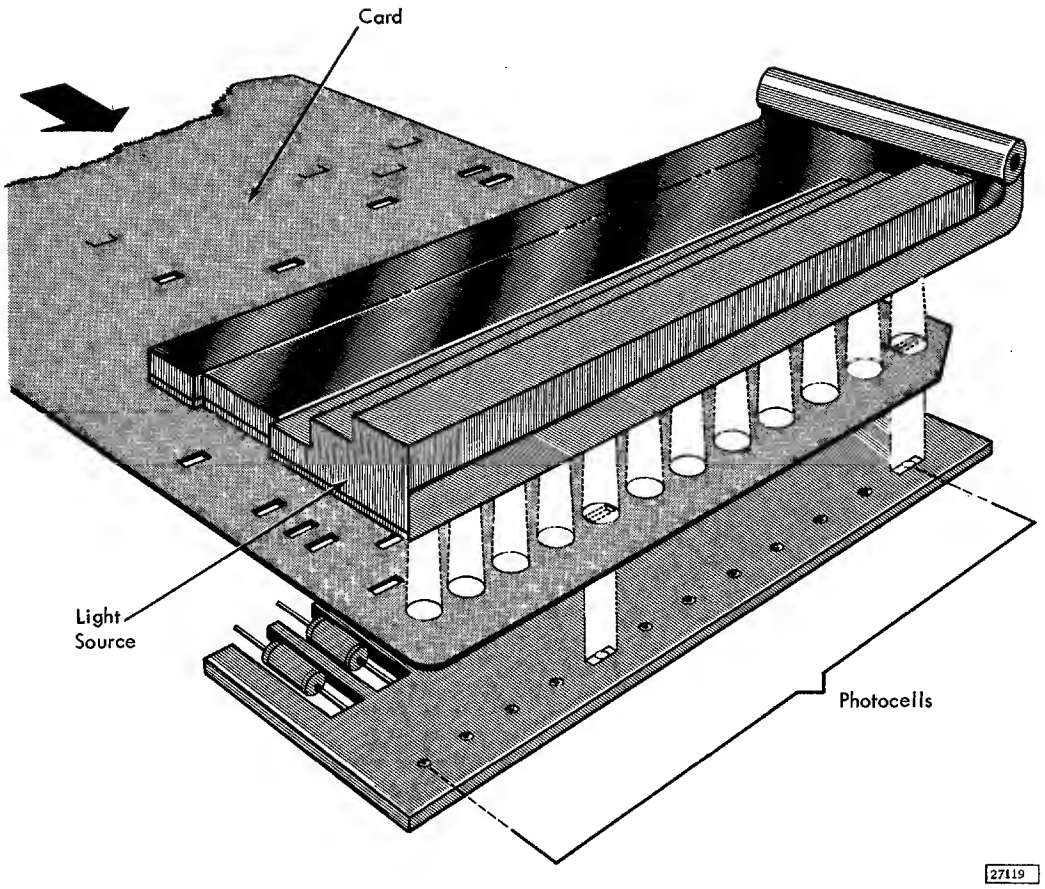


Figure 7-3. Photocell Reading

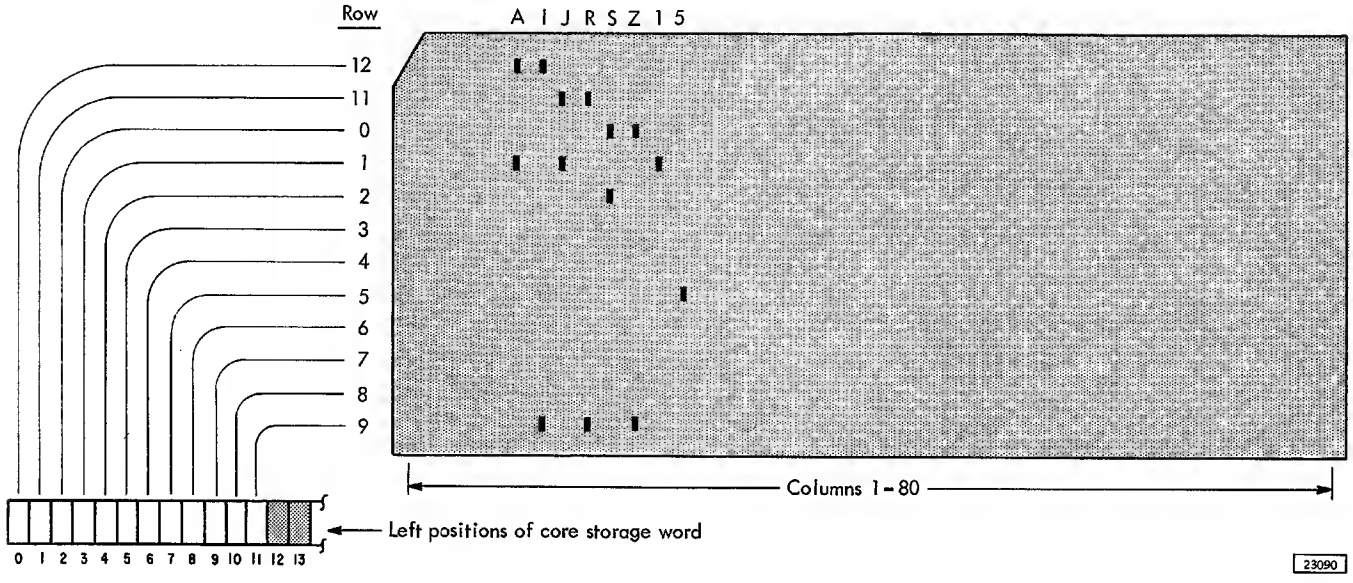


Figure 7-4. Card Code

continue processing cards by placing more cards in the hopper and pressing the start key. Otherwise he can initiate a last-card sequence by pressing the start key without placing cards in the hopper.

When the last-card sequence is entered, the program determines this through the last card indicator in the device status word. This indicator is on while the last card passes the read station. When the start key is pressed without cards in the hopper, the 2501 is placed in the ready condition and the program causes one more feed cycle to be taken to read the last card.

PROGRAM LOAD

After a system reset and the run-in cycle of a load cycle, program load can be initiated by pressing the program load key on the CPU console. This load mode operation causes the load card data to be read and placed in 80 consecutive memory positions beginning at memory position /0000. Figure 7-5 shows the format in which each column is set into core storage. When the load card has passed the read station, the usual interrupt request at the end a feed cycle is blocked. Instead, the CPU T-clock starts, and execution of the instruction just loaded into position /0000 starts.

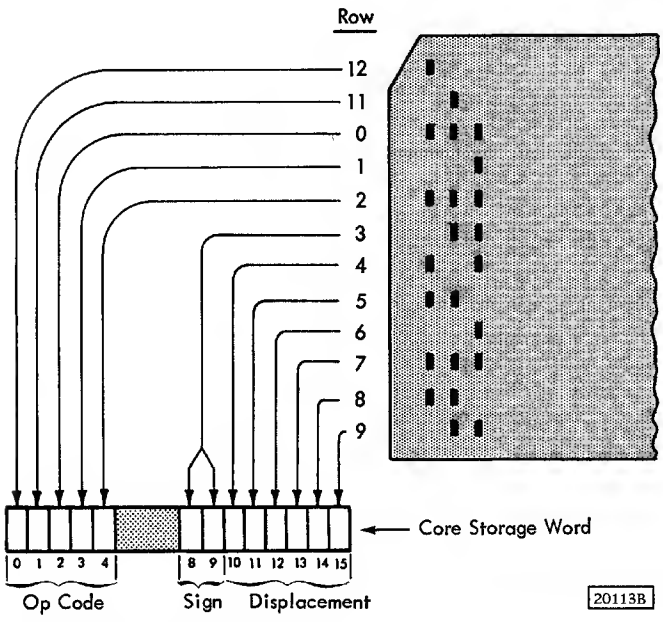


Figure 7-5. Program Load Data Transfer

FUNCTIONAL UNITS

CR READ REGISTER

- Read register contains one CR register FF for each punching row of a card.
- Data enters the register from the solar cells of the 2501.
- Data is checked by comparing the register output with the still-active reading from the 2501.
- Contents of the read register set the CPU B-register during cycle steals.

The 'read bit' lines are activated when the corresponding solar cells in the 2501 are exposed. The lines gate the turn-on of the flip-flops in the read register. Activating the 'CR read register load SP' line sets the register. This sample pulse results from the voltage shift at the start of the column emitter time, only if the 'read error latch' is off.

Register outputs are checked by exclusive OR (OE) circuits against the set gates. At the end of the column emitter pulse, any equal compare bit line that is not active causes the turn-on of the 'read error latch.' The 'read error latch' cannot be turned on after a full word count is reached.

All flip-flops of the read register are turned off (reset) by any of these conditions:

1. DC reset from the CPU.
2. Read initiate and T4.
3. During run-in.
4. Level 3 CS cycle and X6.

CR WORD COUNT REGISTER

- Word count register determines the number of data words that are transferred to the CPU from a card.
- First CS cycle sets the register from the first word of the data table in a programmed read operation.
- First CS cycle forces a word count of 80 in a program load operation.
- Word count register is used as a seven-position binary counter. The value set into it is always the 1's complement of the word count.

- Value in the word count register is stepped by changing the state of the low order position FF.

The value set into the word count register at the start of an operation determines the number of data-transfer CS cycles for that operation. In a programmed read operation the register is reset (all flip-flops turned off) at T4 of the E2 cycle resulting from an initiate read command. Then, at X6 of the first CS cycle, 'load word counter SPD' is activated. The sample pulse turns on those word count register flip-flops gated by B-register positions 9-14 that are off. Thus, the 1's complement is set into the word count register.

In a program load operation, 'word count load bit 9' and 'word count load bit 11' are activated. At register load time, all flip-flops other than 9 and 11 are turned on. The register then must be stepped 80 times to reach a full word count, allowing 80 columns of data to be transferred to the CPU from the load card.

In a programmed read operation, the value in the word count register is not stepped during the first CS cycle. (The register is only loaded during this cycle.) However, in the first CS cycle of a program load operation, the register is loaded at X0 and stepped at the usual time. With the exception of the cycle previously mentioned, the word count register is incremented at X6 of each CS cycle. The increment pulse changes the state of the units position FF. The turning off of any register flip-flop changes the state of the next higher order FF. Thus, the word count register is stepped in the usual binary counter manner.

When all word count register flip-flops are on, ANDing their outputs activates 'full word count.' This line prevents further level 3 CS requests or for data transfer.

CR CORE ADDRESS REGISTER

- Register addresses CPU core storage during level 3 CS cycles.
- Register is reset to 0 (all flip-flops off) at T4 of E2, when the function is initiate read. DC reset also turns off all flip-flops.
- Address word of the IOCC sets this register at T6 of initiate read.
- Register operates as a binary counter, being stepped at the end of X6 in each level 3 CS cycle.

The CR address register, which is used to address storage during all level 3 CS cycles, consists of 15 flip-flops. All positions are turned off at T4 of the E2 cycle that results from an XIO instruction with an IOCC function cycle of 'initiate read.' Then, a T6 pulse activates 'load address SPD' and sets the register to the value presently in the CPU B-register. At this time the B-register contains the address of the first word of the data table (the word count address).

After addressing storage in each CS cycle, the CR address register is stepped at the end of X6. The voltage shift changes the state of the units position FF in the register. Turning off any register flip-flop changes the state of the next higher order FF. Thus, the CR address register is stepped in the usual binary counter manner.

PRINCIPLES OF OPERATION

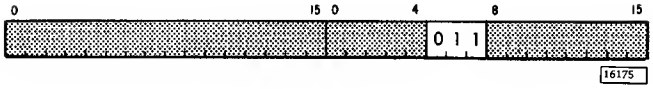
- The 2501 adapter initiates action by the 2501 as the result of an XIO instruction in the CPU program.
- The area code for the 2501 is decimal 9 (01001).
- Function codes that are applicable to the 2501 are:
  Sense interrupt.
  Sense device.
  Initiate read.
- The adapter also controls a program load operation that results from pressing the CPU program load key.
- Maintenance diagrams for the 2501 (FR401, FR411, FR412, FR413, FR501, FR511, and FR512) are in IBM Field Engineering Maintenance Diagrams, 1130 Computing System Features, Y26-4003.
- Timing charts for the 2501 (FR711, FR721, and FR741) are machine logic pages.

SENSE INTERRUPT (011)

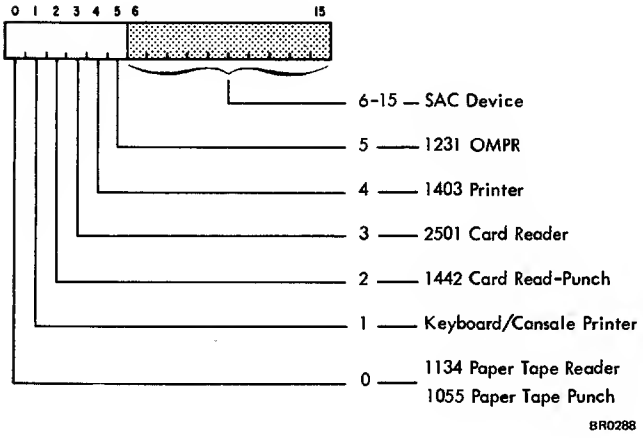
- Sense interrupt sets the interrupt level status word (ILSW), for the presently active interrupt level, into the accumulator of the CPU.
- Area code is not required in the IOCC.
- 2501 interrupts on level 4.

- Maintenance Diagram FR511.

The IOCC for the sense interrupt function is:



An XIO instruction with a function code of sense interrupt activates the 'XIO sense ILSW' line from the CPU. If 'interrupt level 4' is active when the instruction is given, an 'end operation response' activates the 'CR ILSW bit 3.' The ILSW for interrupt level 4 is:



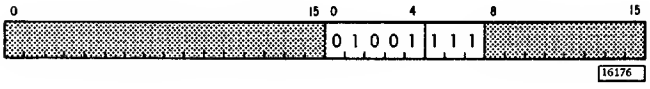
SENSE DEVICE (111)

- Sense device sets the device status word (DSW) for the 2501 adapter and device into the accumulator for the CPU.

- Status conditions in the 2501 result in 1's being set in the DSW during the CPU E2 cycle.

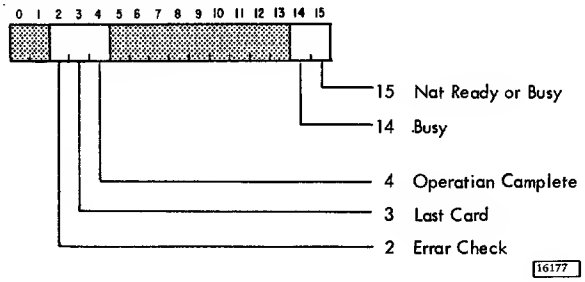
- Maintenance Diagrams FR511, FR512.

The IOCC for the sense device function, specifying the 2501, is:



The CPU activates 'XIO sense device' and 'area 9' during the E2 cycle. These lines create a gate in the adapter for the bits of the DSW. The bits set the B-register, and later in the cycle DSW is transferred to the accumulator by CPU circuits.

Of the status conditions that can set 1's in the DSW of the 2501, only an end operation response (operation complete) causes an interrupt request. The DSW is:



Significance of DSW Bits

Error Check (Bit 2): A 1 in this position indicates that the 'CR error' line is active. This line can be active as a result of a feed check error or a read error. A feed check, which lights the feed check light in the 2501, results from turning on the 'hopper feed check', FL, the 'read feed check' FL, or the 'column emitter check' FL.

A read error activates the 'CR error' line and lights the read check light in the 2501 when the 'read error latch' is on. The 'read error latch' can be turned on by either of these conditions:

1. An equal compare bit line not active.
2. The 'fiber optic test' FL in the 2501 being on on when 'CR column emitter' is active.

Last Card (Bit 3): A 1 in this position indicates that the last card is being fed through the read station. The 'last card latch' is on, having been turned on by activating 'feed allow' while the 'last card trigger' is on.

Operation Complete (Bit 4): A 1 in this position indicates that the 'end operation' FF is on. 'End operation' is turned on by the 'read request' FF turning off.

Busy (Bit 14): A 1 in this position indicates that the 'read request' FF is on. 'Read request' is on from the start of a read operation until the 'feed cycle' FL is turned off. A 1 is also set in the DSW bit position 15.

Busy or Not Ready (Bit 15): A 1 in this position indicates that the 2501 is busy [see "Busy (Bit 14)"] or is not ready. The not ready condition is present when the 'ready' FL is off. The ready indicator in the 2501 is not lit at this time.

The 'ready' FL can be turned on by turning on the 'start' FL while the 'card in preread' FL is on. The 'ready' FL can be turned off by any of these conditions:

1. Power on reset.
2. Pressing the stop key.
3. A read error. See "Error Check (Bit 2)."
4. Hopper empty, except during the last-card sequence.
5. Cards in the hopper during the last-card sequence.
6. Stacker full or cover open while a card is in the preread station. Either of these conditions activates the 'combined attention' line and lights the 2501 attention light.

INITIATE READ (110)

- Initiate read sets the adapter for a read operation.
- Card feeds from the preread station to the stacker.
- Each column is set into the CR register and checked.
- CS level 3 cycles transfer data from the CR-register to core storage via the B-register.
- Word count determines the number of columns of data to be transferred.
- End operation response interrupt level 4 request occurs at the end of the card feed cycle.
- Maintenance Diagrams FR401, FR411, FR412, FR501, FR511, FR512.

To start a read operation, a card must have been run in and the 2501 made ready, and the 2501 must not be busy. Under these conditions, an XIO instruction with the initiate read function code in the IOCC can activate the 'CR read initiate' line.

The IOCC for the initiate read function and the format of the data table used is shown in Figure 706.

Logic flow diagrams FR411, and FR412 describe the read operation in detail, with reference to the I/O operations diagrams FR501, FR511, and FR512. These diagrams show how the following objectives of a read operation are accomplished.

1. At T4 of E2 cycle, clear word count, CR address (cycle steal), and CR (read buffer) registers.
2. At T6 of E2 cycle, load CR address register with word count address from IOCC, and request 1st CS cycle. Also, turn on 'read request' to start card feed cycle.
3. During 1st CS cycle, set word count register with 1's complement of B-register 9 through 15 positions. B-register contains first word of data table (word count) at this time. Step CR address register plus 1 to address of first data word position of data table.
4. Resume CPU program execution until next CS request. Card feed cycle starts. (Card is leaving preread station.)
5. When leading edge of card blocks any read solar cell and trailing edge of card exposes prepread solar cell, magnetize 60 spots on emitter drum in 2501 (record emitter). Thus, column emitter is timed to each card. Magnetized spots combine to provide one emitter pulse per card column.
6. At start of each column emitter pulse, set CR-register from read solar cell outputs.
7. At end of each column emitter pulse, check setting of CR-register. Any unequal comparison of bits allows error sample pulse to turn on 'read error latch,' unless full word count has been reached. Also, same sample pulse causes CS request level 3 unless full word count has been reached.
8. During CS cycle, transfer contents of CR-register to CPU core storage, via B-register. Later, reset CR register, and step word count register

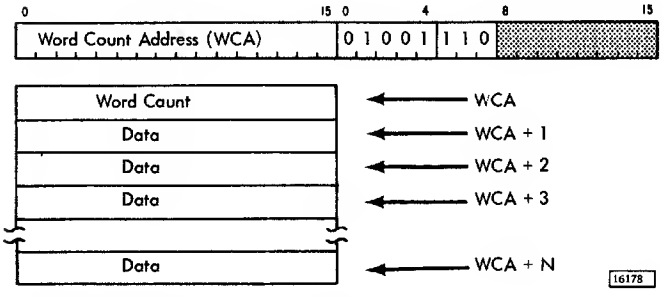


Figure 7-6. IOCC and Data Table (2501 Read)

toward 0 (increment). Also increment CR add address register, which addresses core storage in CS cycle.

9. Continue reading, checking, and cycle stealing for each column until full word count is reached. Then transfer no more data.
10. Continue feeding. At feed CB2 time, turn off 'feed cycle' FL, which turns off 'allow column emitter' and 'read request'. Also at CB2 time erase the 60 spots from the column emitter drum. drum.
11. Turn on 'end operation' FF by turning off 'read request'. Activate level 4 interrupt request, and gate ILSW bit 3 and DSW bit 4.
12. At feed CB3 time, activate erase check circuits.

PROGRAM LOAD

- Program load operation is started by pressing the CPU program load key with the load card in the preread station.

- Operation reads, checks, and cycle steals to transfer data just as in a programmed read operation. Data transfer paths are changed so that each column enters storage as a one-word instruction.

- Word count (0101111) is set into word count register early in first CS cycle. Word count is incremented each CS cycle.

- CR address register starts at /0000 and is incremented for each column, addressing storage each CS cycle.

- Program load blocks the end operation level 4 interrupt request.

- Immediately following the loading of one card, execution of the instruction at location /0000 starts.

- Maintenance Diagrams: FR401, FR411, FR412, FR501, FR511, FR512, and FR741.

Before starting a program load operation, a system DC reset and run-in of the load card are required. Thus, the operation starts with the CR (read) register, the word count register, and the CR address register reset. Pressing the CPU program load key starts the operation, which is similar, in many ways, to a programmed read operation.

Logic flow diagrams FR411 and FR412 and timing chart FR741 show the following major differences between a program load operation and a programmed read operation.

1. Eliminate loading of CR address register (leaving it at /0000). Also eliminate CS cycle that loads word count register. Take first CS cycle when column emitter has caused reading and checking of column 1.
2. Force word count, 0101111, into word count register at X0 of first CS cycle. This allows transfer of 80 columns of data in program load operation.
3. Transfer data in each CS cycle as shown in Figure 7-5.
4. After data from 80 columns has been read, checked, and transferred to CPU, reset IAR and turn off 'program load.' These functions are caused by full word count and CB2.
5. Start CPU T-clock, which had been blocked by program load. Start execution of program from load card.

RUN-IN

- Run-in is started by pressing the start key with cards in the hopper and no card in the preread station.

- Starting the motor and engaging the feed clutch causes a card to be fed to the preread station.

- 'Ready' FL is turned on unless one of the turn-off conditions is present.

- Maintenance Diagrams: FR413, FR501.

Logic flow diagrams FR413 and I/O operation diagram FR501 show details of the run-in operation.

Turning on the 'start' FL with cards in the hopper of the 2501 and no card in the preread station activates 'run in.' 'Run in' is one way of activating the 'execute command' line to the 2501 and to the turn-on of the 'motor' FL. The 'motor' FL output activates the 'motor relay' line to pick the motor relay in the 2501. After 800 ms, the 'CR motor ready' line is activated, the motor should be at operating speed, and the feed CB lines are being activated repeatedly.

Feed CB2 turns on the 'feed allow' FL, and feed CB3 turns on the 'feed cycle' FL. 'Feed allow' and 'feed cycle' energize the hopper magnet and read select magnet in the 2501. Feed CB1 turns off the

'feed allow' FL, deenergizing the magnets, but card motion has started and continues until the next feed latch time.

Near the end of the feed cycle, the card covers card lever 1 photocell, turning on the 'card in preread' FL. The 'start' FL is still on, at this time, so the two conditions turn on the 'ready' FL. By the time CB2 and CB3 have been activated again the run-in is complete and the 2501 is ready.

NONPROCESS RUNOUT

- Pressing the nonprocess runout (NPRO) key on the 2501 starts a feed cycle.
- Card in the preread station is fed to the stacker without processing.
- Hopper must be empty for the NPRO to be effective.
- NPRO causes a CR reset.
- Maintenance Diagrams: FR413, FR501.

Logic flow diagram FR413 and I/O operation diagram FR501 show details of the NPRO operation. In many respects, the NPRO operation is similar to the run-in operation. However, the hopper must be empty to allow an NPRO operation.

Pressing the NPRO key turns off the 'NPRO interlock' FL. Then, with the hopper empty, 'CR reset' can be activated and prevent processing. Unless one of the "start inhibit" conditions is present, pressing the key turns on the 'NPRO' FL. This flip-latch activates the 'execute command' line. The 2501 motor starts, and the card feed starts. The card in the preread station is fed to the stacker.

FEATURES

There are no features for the IBM 2501 Card Reader Adapter.

POWER SUPPLIES AND CONTROL

Power for the IBM 2501 Card Reader Adapter is provided and controlled by the CPU.

CONSOLE AND MAINTENANCE FEATURES

There are two locations in which the CE pluggable indicator cards (P/N 5803975) is plugged. The use of the indicator cards is shown on ALD pages FR011 and FR021. Operator panel lights and keys are described in "Principles of Operation."

INTRODUCTION

FUNCTIONS OF THE IBM 1231 OPTICAL MARK PAGE READER

- The optical mark page reader (OMPR) provides computer input from source documents (data sheets) at a maximum rate of 2,000 documents per hour.
- Document reading is initiated under direct program control.
- Data transfers to the CPU are made one word at a time, using the interrupt request method.
- Data is normally read from the data sheet to the OMPR delay line and from the delay line to the adapter buffer.
- If the contents of the adapter buffer have not been transferred to the CPU, the succeeding data word (or words) is regenerated to the delay line.
- A full page of data (100 words) can be stored in the OMPR delay line.
- The 1231 cannot be installed with an IBM 2501 Card Reader.

The 1231 Optical Mark Page Reader (OMPR) provides for the direct entry of data from source documents into the 1130 Computing System. The source documents can be order, inventory, or any other data marked on the basic OMPR forms (data sheets). These data sheets can contain up to 100 data words arranged in two vertical columns. Each data word consists of two groups of five positioned marks each (see Figure 8-1).

Data is read from the data sheets by a photoelectric read head. The read head consists of 21 photocells. Ten photocells sense data word 1 (odd), ten photocells sense data word 2 (even) and, one photocell senses the timing marks on the right edge of the data sheet. Each horizontal line on the data sheet has two timing marks associated with it (odd, even) to control the read operation. The first timing mark enables the transfer of the odd-numbered data word to sonic delay line in the OMPR and the second timing mark enables the transfer of the even-numbered data word to the sonic delay line (Figure 8-2).

The 1231 OMPR contains two delay lines, one for storing the data from the detail data sheets (data delay line) and a second for storing data from the master and control data sheets (master delay line) (Figure 8-2). When data is to be stored on the master delay line, the operator must use a master data sheet (which has a master mark to the right of the timing marks) or must press the program load pushbutton. If the read station senses a master mark, the ten data words on the data sheet are stored in positions 1 through 10 on the master delay line.

When a master mark is not detected and the program load pushbutton is not pressed, the OMPR stores the detail data from the data sheet on the data delay line in positions 12 through 111 (positions 1 through 11 are not used).

The operation of the master and data delay lines are synchronized by a common clock. Therefore, at any one time both delay lines are at the same word position. (If data is being read into position 12 on the data delay line, the master delay line is regenerating data into position 12.) The synchronous operation of the delay lines permits the control data (master line) to be sensed and the desired control functions to be performed on data prior to the storage of the data on the delay line. The control functions condition circuits in the OMPR which determine if a data word or part of a data word is to be stored and/or if field checking is to be performed. Every data word on a data sheet must have a corresponding control word if the data word is to be stored on the data delay line and transferred to the 1131 CPU.

READ OPERATION

- Marks are sensed on the data sheet by the read station.
- Control data is read from the master delay line and data control conditions are set up in the OMPR.
- The OMPR determines if segment 1, 2, both, or none are to be stored and performs the required field checking on each data word.

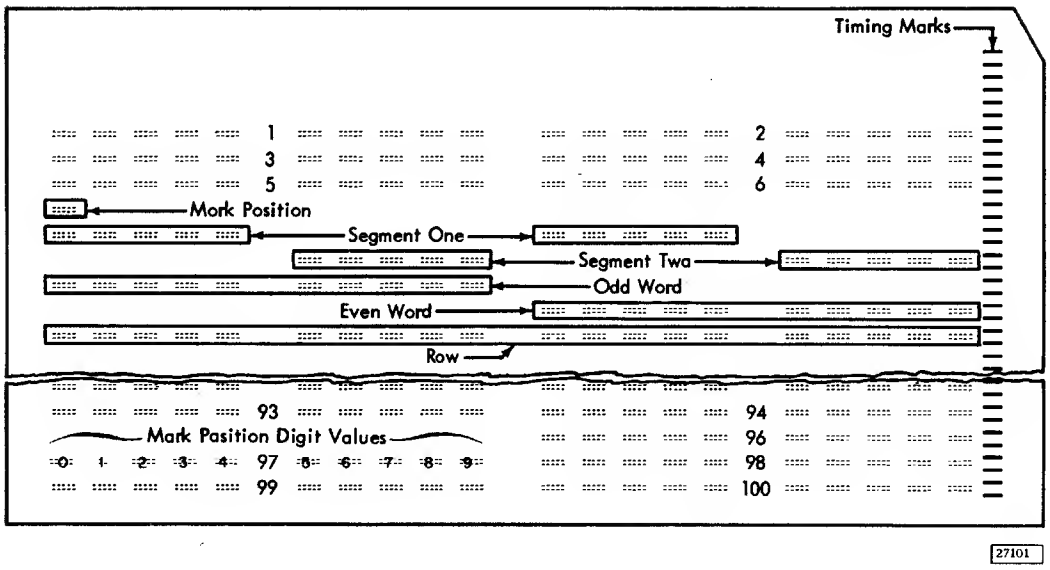


Figure 8-1. Data Sheet Format

- The data word checks are completed and the word is stored (if specified by the controls) on the delay line.

Reading of a data sheet by the OMPR is initiated by an XIO control command from the 1131 CPU. This command is decoded in the adapter and transmitted to the OMPR where it causes the data sheet to move from the hopper to the read station.

As the document moves through the read station, data is read from the document, checked by the control circuits, and stored on the delay line. Each data word is checked individually by the control circuits to determine if the word or a segment of the word is to be stored on the delay line and/or field checking is to be performed. On completion of the checking, the data is stored or destroyed as indicated by the control circuits.

Data Transfer

- Read a data word from the document, perform the checks indicated by the control data and the field check switches.
- Store the data word on the data delay line.
- Transfer data word from the data delay line to the output buffer and generate a service request to the 1231 adapter.
- When the adapter responds with service response, transfer the data word to the adapter.

Data words which are to be transferred to the CPU are cycled through the delay line one or more times. When the data word has cycled through the delay line, the OMPR transfers the data to the output buffer register (if the 1231 adapter is not busy) and generates a service request to the 1231 adapter. On receipt of a service response from the adapter, the OMPR transfers the data word from the output buffer to the adapter (Figure 8-2).

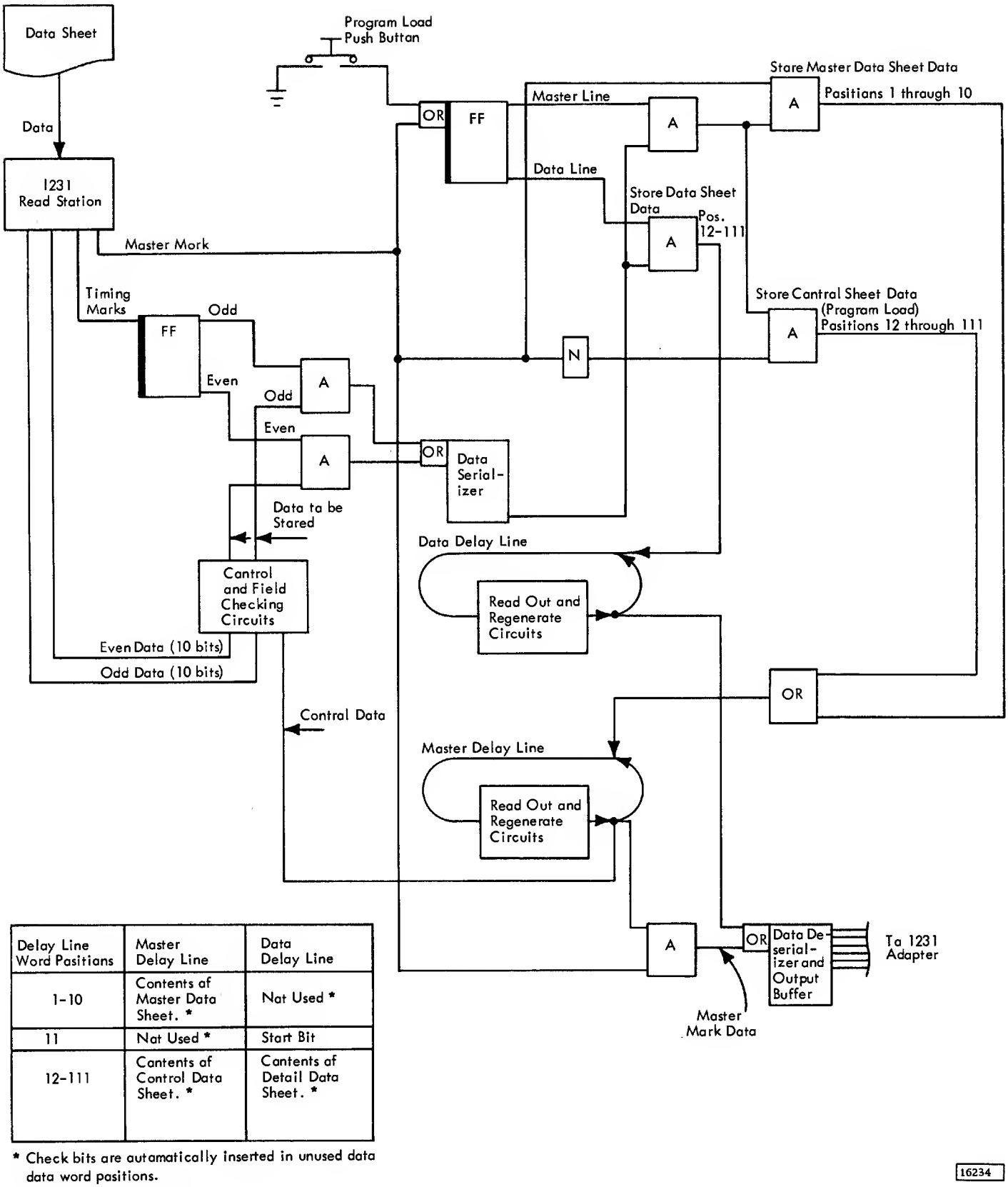
If the CPU has not serviced the adapter by the time the next data word is available from the OMPR, the data transfer to the adapter is inhibited and data words from the delay line are regenerated. However, normally there is no backlog of data on the delay line.

Read Termination

- There are three methods of ending an OMPR read operation:

  1. End of transmission from the OMPR.
  2. I/O disconnect from the 1131 CPU.
  3. Check-stop condition from the OMPR.

- End of transmission and I/O disconnect cause the delay line in the OMPR to be reset (cleared).
- The termination of a read operation allows the OMPR to feed a new document into the read station.



Delay Line Word Pasitians	Master Delay Line	Data Delay Line
1-10	Contents of Master Data Sheet. *	Nat Used *
11	Nat Used *	Start Bit
12-111	Contents of Control Data Sheet. *	Contents of Detail Data Sheet. *

* Check bits are autamatically inserted in unused data data word positions.

Figure 8-2. OMPR Block Diagram

When the last data word stored on the delay line has been transferred to the adapter, the OMPR generates an end of transmission. The end of transmission causes the adapter to generate an operation complete interrupt to the CPU. This interrupt informs the CPU that the contents of this data sheet have been transferred and that the OMPR requires another XIO control command if additional data sheets are to be read.

The I/O disconnect is generated by the CPU when the program has determined that additional data is not required or cannot be stored. This command causes the delay line to be reset and allows the selection of a new data sheet with an XIO control command. The OMPR does not send an end of transmission since the CPU initiated the disconnect.

If a feed check occurs in the OMPR, the OMPR sends a check-stop signal to the adapter. The adapter then generates a check-stop interrupt to notify the CPU that a feed check exists in the OMPR. This interrupt can also be generated by the adapter if a document is being fed and 'OMPR ready' becomes inactive before 'read gate' is generated by the OMPR.

PROGRAMMING

- The operation of the 1231 OMPR is controlled by the program control sheet and XIO commands from the 1131 CPU.
- The program control sheet controls internal OMPR operations and determines which data words are to be transferred to the 1131 CPU.
- The XIO commands control the feeding of data sheets, stacker selection, and adapter functions.

Program Control Sheet

- The program control sheet contains operational controls for the OMPR.
- Control data is marked on a standard data sheet.
- Control data is read into the master delay line by the program load pushbutton.

The program control sheet is a standard data sheet which has been marked with special operational controls in the data areas. Each data word position that is to be transferred to the 1130 CPU must have a corresponding control word stored on the master delay line. These controls are stored in word positions 12 through 111 on the master delay line during the OMPR program load sequence. The control codes are shown in Figure 8-3.

I/O Control Commands

Three XIO commands ('XIO control', 'XIO read', and 'XIO sense device') are used in programming the 1231 OMPR. These commands cause the OMPR to read a document, select the alternate stacker, transfer data to the CPU, transfer the device status word to the CPU, and to disconnect. The OMPR is selected by a device area code of 8. In addition, the 'XIO sense interrupt status word' command is used to determine which device is interrupting on interrupt level 4. The 'XIO sense interrupt' command does not require an area code since this command is used to determine the interrupting device on interrupt levels (such as level 4) which have more than one device connected to them.

The IOCC's are described in detail in "Principles of Operation" for the 1231 (Part 8 of this manual).

FUNCTIONAL UNITS

- The 1231 adapter synchronizes and controls the transfer of data from the OMPR to the CPU.

0	1	2	3	4	5	6	7	8	9	Function
X								X		Store Segment 1
					X			X		Store Segment 2
								X		Store Both Segments
						X				Perform checks indicated by Field I switches
							X			Perform checks indicated by Field II switches
						X	X			Perform checks indicated by Field III switches
X					X			X		Illegal, No data is stored. All other control code combinations are legal and will be performed.

16246

Figure 8-3. OMPR Control Codes

- The major functional units for the 1231 adapter are:
  Page reader controls.
  Data transfer controls.
  Interrupt controls.

- The page reader controls initiate the reading of a document, activate the select stacker, and enable the CPU to disconnect the 1231 OMPR.

- The data transfer controls synchronize the transfer of data from the 1231 to the adapter and from the adapter to the CPU.

- The interrupt controls alert the CPU to the availability of data and to changes in the status of the 1231 and/or the adapter.

- The 1231 operations are performed under direct program control.

PAGE READER CONTROLS

- These controls consist of the 'feed document' flip-flop, the 'feed busy delay' flip-flop, the 'select document' AND, and the 'I/O disconnect' AND.

- The select document, feed, and I/O disconnect functions are initiated by an 'XIO control' IOCC.

- The 'feed document' flip-flop maintains the feed document line to the OMPR until the 'OMPR read gate' starts.

Feed Document and Feed Busy Delay

- The 'feed document' flip-flop causes the OMPR to feed a document from the hopper to the read station.

- An 'XIO control' feed IOCC is required for each document to be read.

- The 'feed document' flip-flop is set by area 8, U-register bit 13, XIO control, OMPR ready, and T6 of the E2 cycle.

- 'Feed busy delay' maintains the feed busy DSW bit to the CPU after the reset of the 'feed document' flip-flop.

- 'Feed busy delay' is set by the 'OMPR read gate' line.

- 'Feed busy delay' is reset at the end of the read response for the first data word transferred to the CPU.

The 'feed document' flip-flop causes the OMPR to feed a document to the read station. This flip-flop is set by a decode of 'XIO control' IOCC with modifier bit 13 at T6 of the E2 cycle (MDM 85-10). When the document enters the read station and the OMPR detects the first timing mark, the OMPR read gate' signal is sent to the adapter.

In the adapter the 'OMPR read gate' is active if the 'check stop enable' FF is set. The 'check stop enable' FF is set when the 'feed document' FF is set. When active, the 'OMPR read gate' resets the 'feed document' flip-flop, sets the 'read operation' and 'feed busy delay' flip-flops, and activates the 'enable select' line. Each of these conditions is indicated to the CPU by bits in the 1231 DSW.

The 'feed busy delay' FF remains on until the first level 4 OMPR interrupt request has been serviced by the CPU. Turning off the 'OMPR read response' FF then turns off 'feed busy delay.'

From the time 'feed document' is turned on until 'feed busy delay' is turned off, the 'OMPR feed busy DSW bit 6' line is active. When the program determines that feed busy is no longer active, it can give a second XIO instruction with a control function and start read modifier. This command again turns on the 'feed document' FF and activates the 'OMPR feed busy DSW bit 6.'

The ability to accept a second 'start read' command before the previous document has been completely read allows maximum input to the CPU.

'Select Document' AND

- This AND causes the document being read to be placed in the alternate stacker.

- The XIO control select document IOCC can be given any time after receipt of the OMPR read gate (enable select).

- The select document AND is conditioned by XIO control, U-register bit 8, and enable select.

The 'select document' AND activates the 'I/O select' signal to the OMPR (MDM 85-10). This signal causes the OMPR to place the document which is now in the read station (or which has just been read within the last 40 ms) in the alternate stacker.

The XIO control select document IOCC is performed only if the IOCC is given when the 'OMPR read gate' is active. The program can determine that 'OMPR read gate' is active by checking the 1231 DSW for the OMPR OK to select DSW bit 5. After detecting the OK-to-select-DSW bit, the program can

issue the select document IOCC. The adapter activates the 'I/O select' line to the OMPR immediately on decoding the XIO control and U-register bit 8 during the E2 cycle of the XIO control IOCC.

I/O Disconnect AND

- The program can terminate the reading of a document before the entire document has been transferred to the CPU.

'XIO control,' 'area 8,' and 'U-register 14' condition two AND's. The output of one sends the 'I/O disconnect' signal to the OMPR, resetting the data delay line. The output of the other AND, when deconditioned, provides the voltage shift that turns off the 'read operation' FF.

DATA TRANSFER AND INTERRUPT CONTROLS

- These controls consist of the 'read operation,' 'OMPR read busy,' 'read response,' 'master mark indicator,' 'end operation,' 'buffer control' flip-flops, data buffer register, and check-stop circuitry.

- With the exception of the data buffer and 'buffer control' flip-flop each flip-flop sets a bit in the DSW and/or generates a request interrupt level 4 to the CPU.

- Causes of interrupts, adapter conditions, and certain OMPR conditions can be set into the DSW by an XIO sense DSW instruction.

- The data buffer register holds the data word in the adapter until the CPU services the interrupt request.

Read Operation FF

- Start of 'OMPR read gate' from the OMPR turns on the 'read operation' FF.

- 'Read operation' generates the DSW bit to the CPU, and gates the setting of the 'end operation,' 'master mark indicator,' 'read busy,' 'read response,' and 'buffer control' flip-flops.

- 'Read operation' is turned off when 'I/O disconnect' ends, 'end operation' FF turns off, or 'I/O check stop gated' is reset.

The 'read operation' flip-flop is turned on by the 'OMPR read gate' and the on output from the 'feed document' flip-flop (MDM 85-10). 'Read operation' sets OMPR read operation DSW bit 14, and enables the adapter to accept data from the OMPR. The 'read operation' flip-flop is turned off by: (1) 'I/O disconnect' (computer cannot accept additional data), (2) the turning off of 'end operation' (the program has serviced the end operation interrupt), or (3) the resetting of 'check stop' FF (the program has serviced a check-stop interrupt).

'OMPR Read Busy' FF

- 'OMPR read busy' is turned on by the end of the master mark or OMPR buffer full line during a read operation.

- 'OMPR read busy' on activates the 'read busy DSW bit 13' to indicate to the CPU that data is available, and turns on the 'read response' flip-flop.

- 'OMPR read busy' is turned off by T6 and XIO read (CPU has accepted the data) or the off output from the 'read operation' flip-flop.

Activating either 'master mark buffer full' or 'OMPR buffer full' activates 'read call' to the OMPR and fires a sample pulse driver (SPD). The SPD output sample pulse (SP) resets the data buffers and turns off the 'buffer control' FF.

Deactivating 'master mark buffer full' or 'OMPR buffer full' turns on the 'OMPR read busy' FF in a read operation. Turning on this FF ends 'read call,' gates the 'read busy DSW bit 13,' and turns on the 'OMPR read response' FF. The read response requests a level 4 interrupt to transfer the contents of the data buffer to the CPU.

After the data is transferred to the B-register during a CPU E3 cycle, T6 turns off the 'OMPR read busy' FF. The E3 cycle occurs in execution of an XIO instruction with a read function code in the IOCC.

'OMPR Read Response' FF

- 'OMPR read response' is turned on by 'read busy' when 'read op' is active.

- 'OMPR read response' is turned off by T6, 'area 8,' and T6 'XIO sense reset 15' if 'B bit 0' is active.

The 'OMPR read response' is turned on to request a level 4 interrupt so that data can be transferred to the CPU. This flip-flop causes a 1 in the bit 5 position of the ILSW and bit 0 position of the DSW when they are sensed during the interrupt level 4 servicing subroutine.

Turning on the 'OMPR read response' FF while the 'buffer control' FF is on turns off all the flip-flops in data buffer B. Thus, all 1's are cleared from data buffer B in a read segment operation.

The 'OMPR read response' flip-flop is reset near the start of the interrupt level 4 servicing subroutine by an XIO sense DSW reset command. This command transfers the DSW to the accumulator at T2 time of the E2 cycle and resets the DSW indicators at T6 time of the E2 cycle.

The first time 'OMPR read response' is turned off in a read operation, the voltage shift turns off the 'feed busy delay.' The program can then give another XIO start read instruction to feed another document.

Data Buffer and 'Buffer Control' FF

- The data buffer consists of 12 flip-flops: 6 flip-flops for word segment 1 (data buffer A) and 6 flip-flops for word segment 2 (data buffer B).
- Each word segment consists of 5 data bits (0 through 4, or 5 through 9) and a check bit (14 or 15).
- The 'buffer control' flip-flop controls the 'set data buffer A' and 'set data buffer B' lines.
- The 'buffer control' flip-flop is complemented by the voltage shift when 'service response' is activated.
- Maintenance Diagram: FD701.

When the OMPR signals 'master mark buffer full' or 'OMPR buffer full,' and the 'OMPR read busy' FF is off, 'read call' is activated. 'Read call' fires an SPD in the adapter and signals the OMPR. The sample pulse from the SPD turns on all flip-flops in both A and B sections of the data buffer. Also, the SP turns the 'buffer control' FF off.

The 'read call' signal to the OMPR gates segment 1 data bits to data buffer A, and causes the OMPR to activate 'OMPR service request.' In the adapter 'OMPR service request' and 'read operation' activate the 'service response' line. Because 'buffer control' is off, 'service response' starts a singleshot (SS) that activates 'set data buffer A.' 'Service response' also turns on 'buffer control,' but this occurs too late to prevent 'set data buffer A.'

Controls in the OMPR determine whether the entire word or only segment 1 is to be read. For a full-word transfer, the OMPR activates 'OMPR service request' a second time. The second 'service request' in the adapter starts the SS that activates 'set data buffer B.' The entire data buffer is now set, ready for transfer to the CPU.

If only segment 1 is to be transferred to the CPU, the OMPR activates 'OMPR service request' only once. When the 'OMPR read response' FF is turned on to request the level 4 interrupt, 'buffer control' remains on. (There is no second 'service response' to turn off 'buffer control.') 'Read response' and 'buffer control' start a SS that turns off all flip-flops in the OMPR buffer B.

End Operation FF

- Flip-flop is turned on by any of three signals from the OMPR.
- 'End operation' causes a level 4 interrupt request.
- Program must turn off the flip-flop in the level 4 servicing subroutine.

The 'read operation' line must be active to gate the turn-on of the 'end operation' FF. 'Read operation' is active while the 'read operation' FF is on or the 90 ms 'timing mark check busy' SS is timing. While gated, the 'end operation' FF can be turned on by a timing mark check signal or a read error signal from the OMPR. An 'OMPR end of transmission' signal can also turn on 'end operation.'

The 'end operation' FF being on gates the OMPR operation complete DSW bit 4. Also, the active 'end operation' line causes an interrupt request, if the 'set read response' line is not active.

Execution of an instruction in the interrupt servicing subroutine must activate the 'XIO sense reset 15' line to the adapter. With 'area 8' and 'B bit 4' also active, 'T6' turns off the 'end operation' FF. Turning off 'end operation' turns off the 'feed busy delay' FF, if it has not been turned off already. Usually, servicing of a read response interrupt has turned off 'feed busy delay.'

Master Mark Indicator FF

- The 'master mark indicator' flip-flop is turned when the 'master mark buffer full' line is activated by the OMPR during a read operation.
- The 'master mark indicator' flip-flop sets DSW bit 3 which indicates that the data being transferred is master mark data.

- Flip-flop is turned off by the deactivation of the 'read operation' line.

The 'master mark indicator' FF is turned on for the transfer of the first master mark data word from OMPR to the CPU. Activating 'master mark buffer full' turns on the 'master mark indicator' FF, if the turn-on is gated by 'read operation.'

In 1130 operation the OMPR transfers the master mark data to the CPU only once, and always as the first data sheet. The data sheets which follow the master data sheet use the data transferred from the master data sheet.

The master mark indicator flip-flop is reset at the end of the master mark data sheet read operation by turning off the 'read operation' FF.

Check-Stop Circuits

- The check-stop circuitry consists of two flip-flops and one flip-latch: 'check stop enable' FF, 'OMPR check stop' FF, and 'check stop interrupt request' FL.

- A 'check stop interrupt request' signals the CPU that a feed error has occurred in the OMPR.

- The program must reset the check-stop condition in the adapter by issuing an XIO sense DSW with reset.

The setting of the feed-check indicator in the OMPR also sends an 'OMPR check stop' signal to the adapter. The 'check stop enable' FF must be on to gate this signal to the 'OMPR check stop' FF after a 300 nano-second delay. The 'check stop enable' FF is set at the same time that 'feed document' FF is set by an XIO control and area 8 with U-reg bit 13 active and OMPR ready.

When the 'OMPR check stop' FF is turned on it sets the 'check stop interrupt request' FL, causing a level 4 interrupt. A sense DSW then sets the OMPR check-stop DSW bit 10. The 'check stop interrupt request' FL can also be set while feeding a document if the OMPR loses ready before an OMPR read gate is generated. To reset the 'check stop interrupt request' FL, the program must issue an XIO sense DSW with reset. This instruction activates 'XIO sense reset 15' which with 'area 8', 'T6', and the active 'B bit 10' resets the 'check stop enable' FF. Turning off the 'check stop enable' FF unlatches the 'check stop interrupt request' FL. The check-stop signal from the OMPR cannot be deactivated until the feed check is cleared in the 1231.

PRINCIPLES OF OPERATION

- OMPR operations are started by XIO instructions in the CPU program.

- Area code for the OMPR is decimal 8 (01000).

- Function codes that are applicable to the 1231 are:
  Sense interrupt.
  Sense device.
  Control.
  Read.

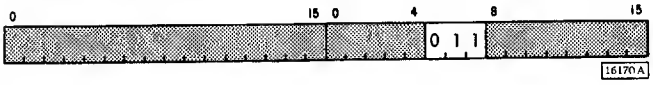
- Modifiers further define the operation resulting from a control function code in the IOCC.

SENSE INTERRUPT (011)

- Sense interrupt sets the ILSW for the active interrupt level in the CPU accumulator.

- OMPR interrupts set a 1 in position 5 of the ILSW for level 4.

The sense interrupt function code in the IOCC of an XIO instruction sets an ILSW in the accumulator of the CPU. The ILSW set is the one for the interrupt level that is active when the instruction is given. The device is not known so the area code is not required in the IOCC:



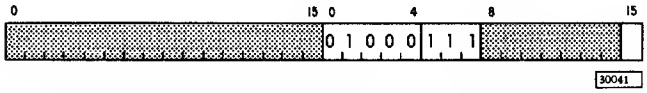
Decoding of the IOCC activates 'XIO sense ILSW' to all adapters. If 'interrupt level 4' is also active, and the OMPR has caused the interrupt, 'OMPR ILSW bit 5' is activated. One of the following conditions in the OMPR will cause an interrupt request: read response, end operation if read busy is off, timing mark error, read error, or check stop.

SENSE DEVICE (111)

- Sense device sets the device status word (DSW) in the accumulator of the CPU.

- Status conditions in the OMPR result in 1's being set in the DSW during the CPU E2 cycle.

An XIO instruction with a sense device function code in the IOCC causes the DSW to be set in the CPU accumulator during the E2 cycle. The IOCC is:



The DSW for the 1231 is shown in Figure 8-4. The conditions which set read response or operation complete response also cause level 4 interrupt requests.

Decoding the IOCC activates 'XIO sense device' and 'area 8' lines. Together these lines gate status conditions via the I/O bus to the B-register for transfer to the accumulator during E2.

Significance of DSW Bits

Read Response (Bit 0): A 1 in this position indicates that the 'OMPR read response' FF is on. Data is in the adapter data buffer ready for transfer to the CPU.

Timing Mark Error (Bit 1): A 1 in this on position indicates that the 'OMPR timing mark check' line from the OMPR is signaling a timing mark error. If 'read operation' is active when the adapter receives this signal, the signal also turns on 'end operation.' The DSW position 4 is also set to 1.

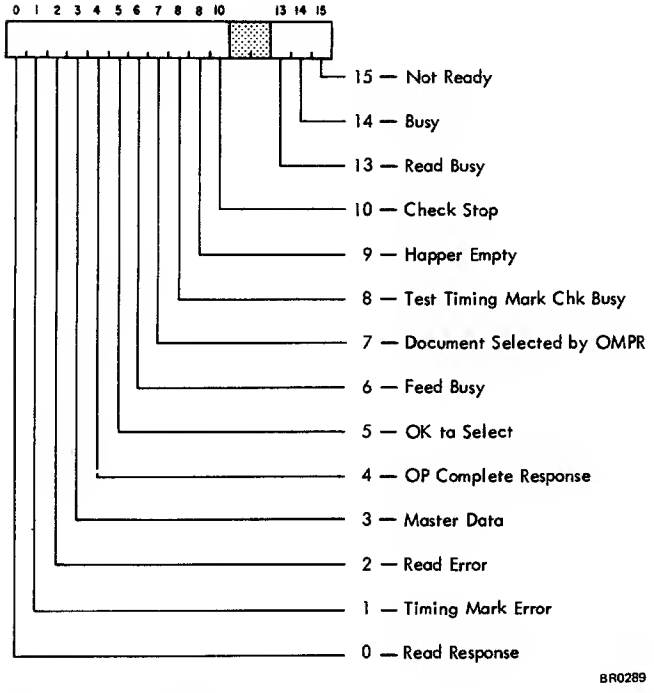


Figure 8-4. Device Status Word

The timing mark error indicator is dependent upon the settings of two switches on the OMPR: timing mark check switch and control timing mark switch. The timing mark check switch is an 11-position rotary switch. It has an off position and ten positions labeled 0 through 9. In the off position, no checking is performed. If checking is desired, the switch is placed on the digit corresponding to the units value of the number of timing marks on the documents. The control timing mark switch has two positions, labeled YES and NO. The no position is used for documents having the normal number of tim timing marks (100 or less); the yes position is used for documents having 106 timing marks.

Read Error (Bit 2): A 1 in this position indicates that the 'OMPR read error' line from the OMPR is signaling a read error. If 'read operation' is active when the adapter receives this signal, the signal also turns on 'end operation.' Then DSW position 4 is also set to 1.

The OMPR generates a read error if a parity error (even count) is detected, or if an overrun condition is detected, or if no bits are entered onto one of the delay lines while reading either a data sheet or a control sheet. The OMPR also signals not ready and causes a 1 to be set in position 15 of the DSW. The OMPR clears the delay line storage so that it is not necessary for the program to give an I/O disconnect.

Master Data (Bit 3): A 1 in this position indicates that the 'master mark indicator' FF is on. The 'master mark buffer full' signal from the OMPR turns on this flip-flop.

A master data subroutine places the master data in a reserved core storage area. The indicator does not come on if the master mark switch on the OMPR is off.

Operation Complete Response (Bit 4): A 1 in this position indicates that the 'end operation' FF is on. The action of this flip-flop is described in "Functional Units" -- "Data Transfer and Interrupt Controls."

OK to Select (Bit 5): A 1 in this position indicates that the 'enable select' line is active. 'Enable select' becomes active at the start of 'OMPR read gate' and remains active until the 'select' SS times out. This is approximately 40 ms after the end of 'OMPR read gate.'

Feed Busy (Bit 6): A 1 in this position indicates that either the 'feed document' FF or the 'feed busy delay' FF is on. One or the other is on from the time the 'start read' is given until 'OMPR read response' is turned off in servicing the first interrupt request.

Document Selected by OMPR (Bit 7): A 1 in this position indicates that the OMPR has activated the 'OMPR auto select' line. A document is being fed to the select pocket without a select instruction. This is caused by either a mark count reject or data uncertainty as determined by the setting of the field checking switches and the program control sheet. Document feeding is not inhibited. When this indicator is turned on, the delay line storage is cleared of data and the transfer to the processor is terminated. The operator must be flagged by the program when this has happened. If the next feed command has been issued, it is necessary to refeed two documents. If the document selected indicator is turned on and serviced before the next feed command, only the top sheet in the select stacker need be processed. Data should not be processed if this indicator is on.

Test Timing Mark Check Busy (Bit 8): A 1 in this position indicates that 'OMPR read gate' is active or the 'timing mark check busy' SS is timing. The singleshot starts at the end of 'OMPR read gate' and times out 90 ms later.

If the control timing mark switch is set to YES, the timing mark check is not made until up to 90 ms after read gate goes off. If this indicator is to be tested, data processing should not take place until the indicator turns off.

Hopper Empty (Bit 9): A 1 in this position indicates that the 'OMPR hopper empty' line is active. When this line is active, the OMPR deactivates the 'OMPR ready' line, and a 1 is set in DSW position 15.

Check-Stop (Bit 10): A 1 in this position indicates that a feed error in the OMPR has caused a check-stop interrupt request. To reset this request, the program must provide for a reset when sensing for this bit. Manual intervention is also required at the OMPR to clear the feed check condition.

Read Busy (Bit 13): A 1 in this position indicates that the 'OMPR read busy' FF is on. Loading the adapter buffer turns on the flip-flop, and transferring the data to the CPU by an instruction ('read') turns the flip-flop off.

Busy (Bit 14): A1 in this position indicates that the 'read operation' FF is on (a document is being read). The start of 'OMPR read gate' turns on this flip-flop. Three conditions can turn it off:

1. Turning off the 'end operation' FF in servicing the operation complete interrupt.
2. Performing the I/O disconnect function of an 'XIO control' command.
3. Turning off the 'OMPR check stop' FF in servicing the check-stop interrupt request.

Not Ready (Bit 15): A 1 in this position indicates that the OMPR is not activating the 'OMPR ready' line to the adapter. All the following conditions are necessary for the OMPR to maintain ready:

1. Power on.
2. Off-line/on-line switch set to ON-LINE.
3. Control sheet loaded.
4. Documents in hopper.
5. No read or feed errors.
6. Start key pressed after loading the control sheet and turning off the program load light.

Sense Reset

Modifier bit 15 = 1 in the IOCC of a sense device command activates the CPU 'XIO sense reset 15' line to the adapter. This line turns off the 'OMPR read response' FF if the 'B bit 0' is active (a 1 in DSW bit 0 position). The same line can turn off the 'end operation' FF if 'B bit 4' is active (a 1 in DSW bit 4 position).

CONTROL (100)

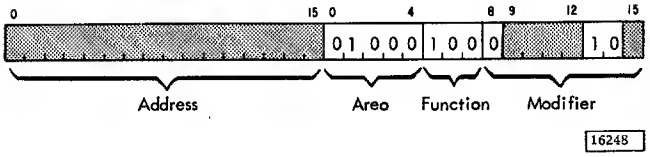
- Control function code in the IOCC of an XIO instruction causes the OMPR to perform the operation specified by the modifier bits 8, 13, and 14.
- Modifier 13 causes a document to feed through the read station.
- Modifier 15 causes the OMPR to stop transferring data to the CPU.
- Modifier 8 causes the document in the read station or leaving the read station to enter the select (alternate) stacker.

During the E2 cycle in the CPU, decoding the IOCC activates the 'XIO control,' 'area 8,' and 'U-register (8, 13, or 14)' lines. These lines to the adapter start operations selected by the U-register line that is active. The U-register contains the control word of the IOCC; so modifier bits activate the corresponding U-register lines.

Start Read (Bit 13)

- Start read feeds a document through the read station.
- Data that is read enters the delay line in the OMPR, as determined by the controls set up by the control sheet and by the OMPR switches.
- Data is transferred to the adapter data buffers A and (if full word) to data buffer B.
- Interrupt level 4 is requested to transfer data to CPU core storage.
- Maintenance Diagrams: 85-10, FD701.

The IOCC for the start read function is:



This command causes the document to move through the read station. Data is collected and placed on the delay line as determined by the control sheet and switch settings. As soon as the first word programmed for output is placed on the delay line, it is made available to the processor.

The CPU decodes the IOCC and activates the 'XIO control,' 'area 8,' and 'U-register 13' lines, Then T6 turns on the 'feed document' FF, starting a document feed cycle. Under control of OMPR timing, the 1231 activates the 'OMPR read gate.' The start of this signal turns off 'feed document' and turns on the 'read operation' FF.

During the read operation, the OMPR sets a word of data from the data sheet to the delay line. Then the OMPR activates the 'OMPR buffer full' line to the adapter, activating the 'read call' line. 'Read call' activates an SPD, and the sample pulse turns on all flip-flops in data buffers A and B. The sample pulse also ensures that the 'buffer control' FF is off at this time.

The 'read call' signal to the 1231 causes the 1231 to return an 'OMPR service request' signal. The OMPR gates a segment of data to the adapter, and 'OMPR service request' activates 'service response' in the adapter. 'Buffer control' is off at the time of the first 'service response;' so the 'set data buffer A' pulse is activated. Thus the first segment of data sets the data buffer A. (A data 0 from the delay line turns off the buffer FF; a data 1 leaves the FF on.)

Controls in the OMPR, established by the control sheet, determine whether or not the second segment is to be read. If the second segment is to be read, the OMPR activates a second 'OMPR service request.' Because the 'buffer control' FF was turned on by the first 'service response,' the second 'service response' sets data buffer B.

The OMPR deactivates the 'OMPR buffer full' line after setting the data buffer register(s). Deactivating 'OMPR buffer full' turns on 'OMPR read busy,' activating 'set read response.' Turning on the 'OMPR read response' FF activates lines to:

1. Gate OMPR read response DSW bit 0.
2. Gate OMPR ILSW bit 5.
3. Cause an OMPR request interrupt level 4.

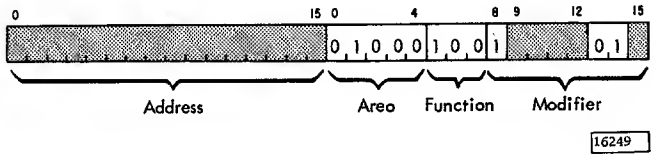
Also, if 'buffer control' is on, 'read response' turns off all flip-flops in data buffer B. 'Buffer control' is on at this time, if only one segment is to be read.

Data is transferred to the CPU from the data buffers by execution of an 'XIO read' command in the level 4 interrupt servicing subroutine.

I/O Disconnect (Bit 14)

- I/O disconnect allows the program to discontinue a read operation before the entire document has passed the read station.

The IOCC for I/O disconnect is:



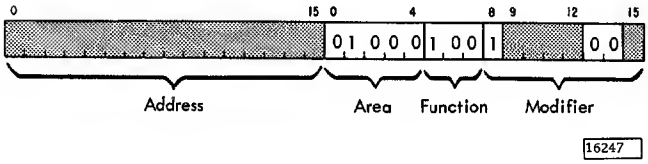
This command signals the OMPR that no more data is desired. This causes the OMPR to terminate the read operation and clear the delay line storage. This command should be given to prevent a read (overrun) error on the next document if all data from the previous document is not cleared from the delay line storage.

The CPU decodes the IOCC and activates the 'XIO control,' 'area 8,' and 'U-register 14' lines. In the adapter, these lines condition two AND's. One activates the 'I/O disconnect' line to the OMPR. The voltage shift when the second AND is deconditioned turns off the 'read operation' FF.

Select Stacker (Bit 8)

- Select stacker causes the document in the read station or just leaving the read station to enter the select (alternate) stacker.

The IOCC for the select stacker command is:

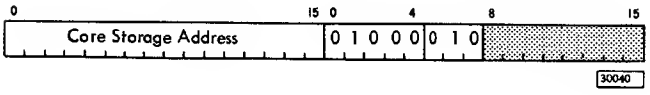


The CPU decodes the IOCC and activates the 'XIO control,' 'area 8,' and 'U-register 8' lines. These lines can activate the 'select document' line to the OMPR only if 'enable select' is also active. 'Enable select' is active from the start of 'OMPR read gate' until the 'select' SS times out 40 ms after the end of 'OMPR read gate.'

READ (010)

- Read function causes data transfer from the data buffer registers to CPU core storage via the B-register.
- Command appears in the interrupt level 4 servicing subroutine.

The IOCC for the read command is:



The CPU decodes the IOCC and activates the 'XIO read' and 'area 8' lines. These lines combine to activate the 'OMPR entry gate' lines in the adapters. One 'OMPR entry gate' line gates the output of data buffer registers A and B to the CPU B-register. The transfer is made during the E3 cycle, timed by the CPU.

The second 'OMPR entry gate' line gates the turn-off of the 'OMPR read busy' FF. After the data transfer in the E3 cycle, T6 turns off 'OMPR read busy.'

FEATURES

There are no features available for the IBM 1231 Optical Mark Page Reader adapter.

POWER SUPPLIES AND CONTROL

Power for the IBM 1231 Optical Mark Page Reader adapter is provided and controlled by the CPU. However, the 1231 device requires its own power source (208/230V).

CONSOLE AND MAINTENANCE FEATURES

There are no console and maintenance features in the IBM 1231 Optical Mark Page Reader.

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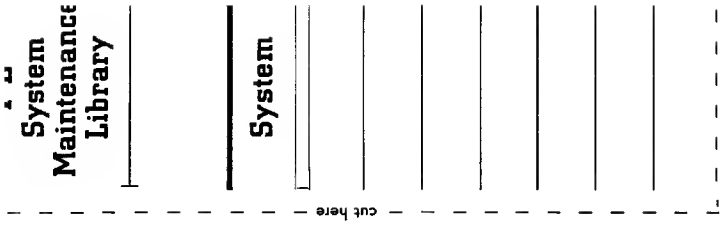

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